Lithography Workshop 2016

The Hapuna Resort

Kamuela, HI

November 6 – 10, 2016

Welcome to the 24th Lithography Workshop!

With the support of its members, the Lithography Workshop has sponsored a unique program which is carefully designed to cover the latest lithography-related advancements to benefit all participants in their field of expertise. The Workshop held its first meeting in Lake Placid, New York in 1981. The 2015 Workshop was the 23rd in a series of meetings that span 34 years promoting the continuing evolution of lithography. The speakers at the Workshop are selected by invitation and represent a broad range of disciplines and covering a wide array of different lithography approaches and requirements. The Workshop is limited to 150 participants.

The Workshop is modeled to be similar to a "Gordon-Research" meeting but with the intent of addressing more immediate issues facing the lithography community within the next few years. The attendees of the Workshop share recent advances and knowledge in lithography with others in the community. The Workshop provides an environment where leading researchers from various disciplines can share their thoughts and ideas. A primary intent is to provide an arena for stimulating debate and the meeting schedule is designed to provide the attendees time for side-meetings and discussions. The Workshop has historically focused on leading-edge semiconductor applications, but has also addressed the challenging lithography needs of flat panel displays, memory devices and 3-dimensional device integration.

This is an opportunity for attendees to meet with world-renown investigators and discuss topics of mutual interest. The Workshop format is intended to provide an atmosphere for in-depth discussions of the invited and poster papers presented. This is accomplished by providing time for extensive questions and answers after each paper, during the poster programs and during group meetings. This year, we will continue with opportunities to present, late-breaking topics of interest. As in the past, there will be no formal proceedings, picture taking, audio or video recording of the Workshop presentations. The technical sessions have been scheduled for mornings and evenings, with time for meetings between attendees and authors during the afternoon. Both invited and late breaking contributing Poster papers will be presented during the evening receptions, prior to the evening oral papers. Please see the Meeting's schedule of events for more information.

The Executive Committee is arranging a program that we believe you will find intellectually stimulating and challenging. Putting together a meeting such as this required the contributions of many people. We are especially thankful to the Technical Program Chairpersons and the Session Chairs who have put together the program. This year, the Technical Program Chair is Dr. Martha Sanchez. Each talk is invited and each speaker is recognized for his/her outstanding work in their field.

We hope that you will avail yourself to all the sessions and functions that the organizers have planned. The Executive Committee welcomes your comments and suggestions to better serve the lithography community.

The Lithography Workshop is very grateful to its sponsors, without whom, we would not be able to continue running the meeting. The LOGOs of our 2016 sponsors are shown on the back cover.

Vivek Singh, Ph.D. President of the Executive Committee

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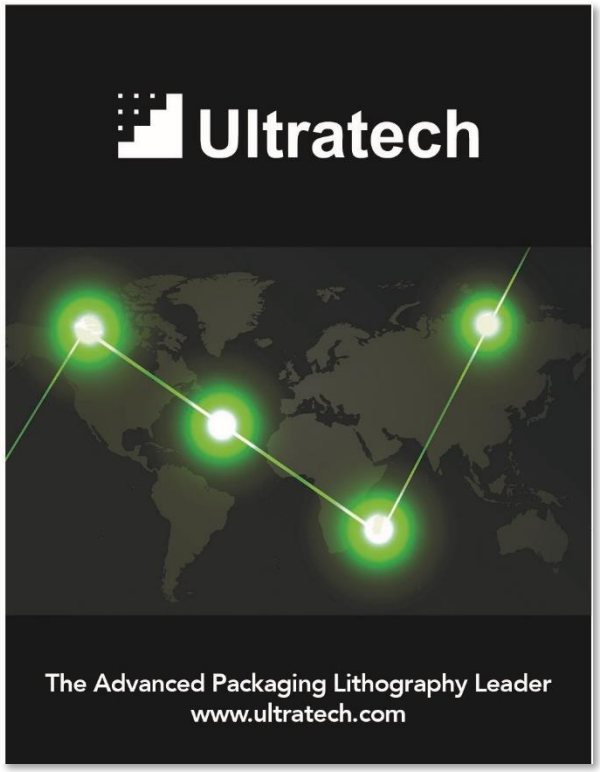

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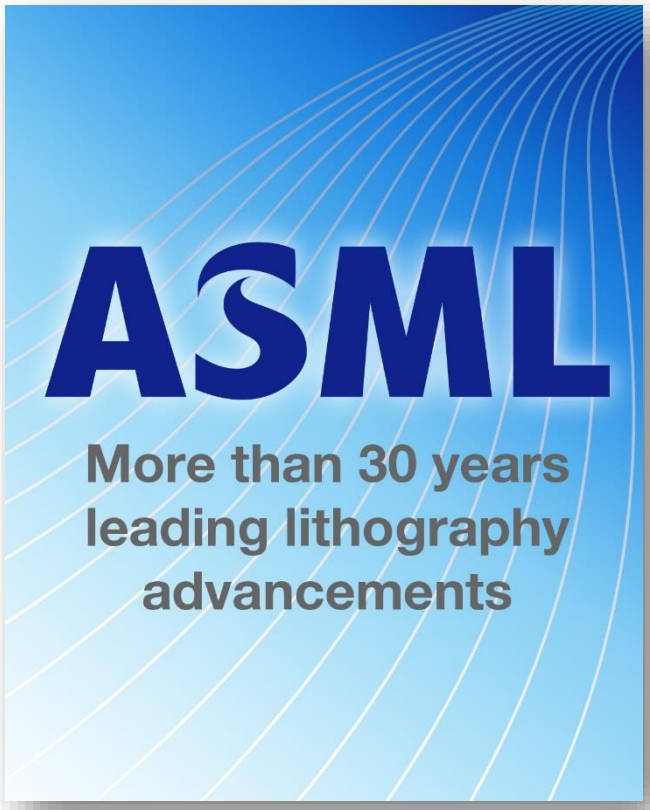

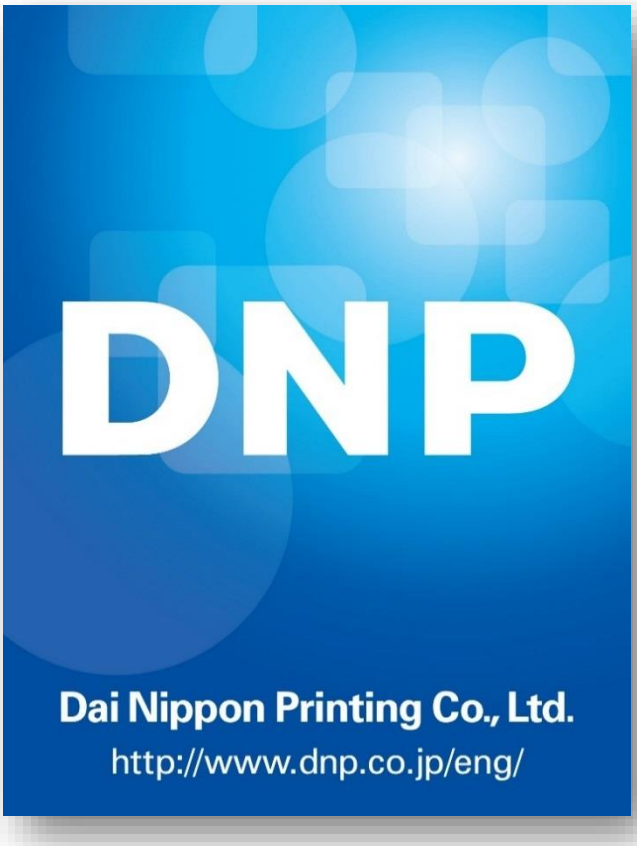

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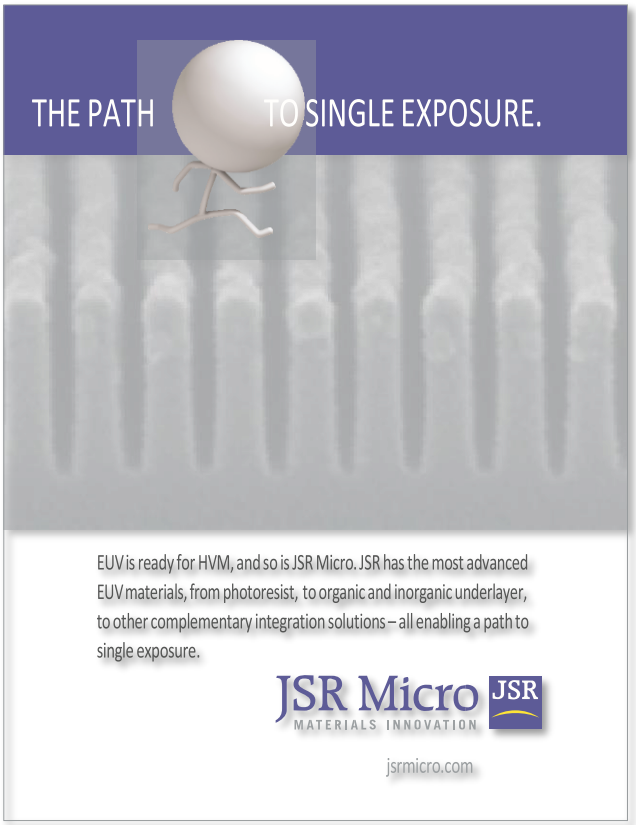

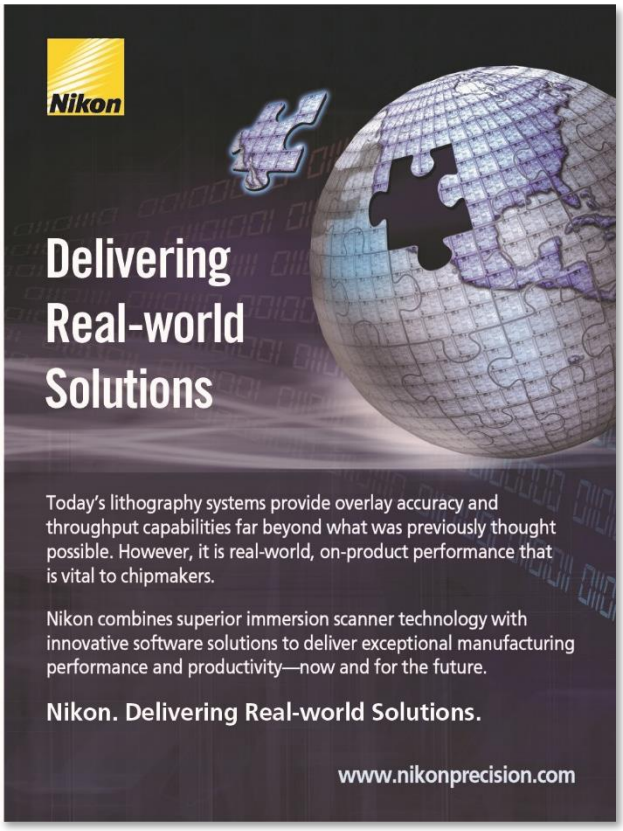

The Executive Committee

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Technical Program Chairs

Martha Sanchez
IBM Corporation

Topical Chairs

	Session	Session Chairs
1	Plenary	**Martha Sanchez (IBM)**
2	Design and Device Technology	**Luigi Capodieci (KnotPrime Inc)** **Da Yang (QCT)** **John Sturtevant (Mentor Graphics)**
3	193i extension and multiple patterning	**Carlos Fonseca (TEL)** **Richard Schenker (Intel)** **Donis Flagello (Nikon)**
4	EUV	**P. Naulleau (LBNL)** **Geert Vandenberghe (imec)** **Bill Arnold (ASML)**
5	Maskless technology	**Deirdre Olynick (MF)** **Alan Brodie (KLA-Tencor)** **Marco Wieland (Mapper)**
6	DSA	**Roel Gronheid (imec)** **Mark Somervell (TEL)**
7	Advanced materials and processes for lithography	**Chris Ober (Cornell)** **Ralph Dammel (EMD Performance Materials)**
8	Computational Lithography	**Bob Socha (ASML)** **Andres Torres (Mentor Graphics)** **Kevin Lucas (Synopsys)**
9	Patterning at 5nm and below	**Pat Martin (Applied Materials)** **Martin Brukhardt (IBM)**
10	Novel litho	**Bruce Smith (RIT)** **John Petersen (Periodic Structures)** **Doug Resnick (Canon)**
11	Non-IC applications	**S. Wind (Columbia)** **M. Rothschild (MITLL)** **D. Pappas (NIST)**
12	Metrology	**Chris Mack (GS)** **Alain Diebold (SUNY CNSE)** **Alex Liddle (NIST)**

SCHEDULE OF EVENTS

Time	Sunday	Monday	Tuesday	Wednesday	Thursday	Time
7:00 AM		7:00 - 8:00 Breakfast (Breezeway)	7:00 - 8:00 Breakfast (Breezeway)	7:00 - 8:00 Breakfast (Breezeway)	7:00 - 8:00 Breakfast (Breezeway)	7:00 AM
7:30 AM						7:30 AM
8:00 AM		8:00 - 10:05 Registration & Technical Session 1 (Makai Salon)	8:00 - 10:05 Registration & Technical Session 4 (Makai Salon)	8:00 - 10:05 Registration & Technical Session 7 (Makai Salon)	8:00 - 10:05 Technical Session 9 (Makai Salon)	8:00 AM
8:30 AM						8:30 AM
9:00 AM						9:00 AM
9:30 AM						9:30 AM
10:00 AM		Break	Break	Break	Break	10:00 AM
10:30 AM		10:35 - 12:40 Technical Session 2 (Makai Salon)	10:35 - 12:40 Technical Session 5 (Makai Salon)	10:35 - 12:40 Technical Session 8 (Makai Salon)	10:35 - 12:40 Technical Session 10 (Makai Salon)	10:30 AM
11:00 AM						11:00 AM
11:30 AM						11:30 AM
12:00 PM						12:00 PM
12:30 PM						12:30 PM
1:00 PM		12:40 - 1:40 PM Lunch provided (Ocean Lawn)	Networking time	Networking time	12:40 - 1:40 Lunch provided (Breezeway)	1:00 PM
1:30 PM						1:30 PM
2:00 PM		Networking time			1:40 - 2:55 Technical Session 11 (Makai Salon)	2:00 PM
2:30 PM				2:30 - 4:40 Technical Session 8B (Makai Salon)		2:30 PM
3:00 PM					Break	3:00 PM
3:30 PM						3:30 PM
4:00 PM					3:25 - 5:00 Technical Session 12 (Makai Salon)	4:00 PM
4:30 PM						4:30 PM
5:00 PM	Registration starts at 5:00 (Coast Grille)	5:00 - 7:00 Poster Session (Breezeway) 5:30 - 7:00 Posters & Reception	5:00 - 7:00 Poster Session (Breezeway) 5:30 - 7:00 Posters & Reception	Networking time		5:00 PM
5:30 PM						5:30 PM
6:00 PM	6:00 - 9:00 Reception (Coast Grille)					6:00 PM
6:30 PM						6:30 PM
7:00 PM		7:00 - 9:30 Technical Session 3 (Makai Salon)	7:00 - 9:30 Technical Session 6 (Makai Salon)	7:00 - 9:00 Reception & Banquet (Ocean Terrace restaurant)		7:00 PM
7:30 PM						7:30 PM
8:00 PM						8:00 PM
8:30 PM						8:30 PM
9:00 PM						9:00 PM
9:30 PM						9:30 PM

Schedule of Presentations
Monday, November 7, 2016

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	9:15 – 9:40 AM	Greg Rechtsteiner (Cymer)	Effects of DUV light source tunable bandwidth on imaging performance	17
	9:40 – 10:05 AM	Eric Hendrickx (imec)	EUV insertion possibilities for N7 and N5 technology nodes	18
	10:05 – 10:35 AM	BREAK		
Session 2	10:35 – 11:00 AM	Ankit Vora (IBM Research Almaden)	Topcoat-free Strategies for Orientation Control of All-organic High-χ Block Copolymers	20
	11:00 – 11:25 AM	Michael Thompson (Cornell Univ. / JSR)	Kinetics of BCP segregation and DSA alignment during millisecond spike annealing	22
	11:25 – 11:50 AM	Nihar Monhanty (TEL Technology Center)	Patterning when variability rules the roost	23
	11:50 – 12:15 PM	Hiroshi Matsumoto (NuFlare Technology)	Multi-beam mask writer MBM-1000	24
	12:15 – 12:40 PM	Keita Sakai (Canon)	A Review of Nanoimprint Wafer and Mask Tool Progress and Status for High Volume Semiconductor Manufacturing	25
	12:40 PM	**Lunch provided**		
	5:00 – 7:00 PM	**Poster Session**		-
	5:30 – 7:00 PM	**Food, Drinks and Posters**		-
Session 3	7:00 – 7:25 PM	Qi-Huo Wei (Kent State / Liquid Crystal Inst.)	Projection Photo Patterning Molecular Orientations in Liquid Crystals by Using Novel Plasmonic Metamasks	27
	7:25 – 7:50 PM	Hiroshi Fukuda (Hitachi High Technology)	Electron beam-based metrology and inspection, overcoming the limitation of scaling, variability, and productivity	28
	7:50 – 8:15 PM	Mike Rieger (Synopsys)	Patterning for advanced integrated devices	29
	8:15 – 8:40 PM	Vito Dai (Motivo)	Physical Design Characterization and Optimization with Graph-based Search, Advanced Analytics and Machine Learning	30
	8:40 – 9:05 PM	Tatsuhiko Higashiki (Toshiba)	Progress and challenges in Imprint Lithography	31
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Schedule of Presentations
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	11:00 – 11:25 AM	Naoya Hayashi (DNP)	EUV masks	41
	11:25 – 11:50 AM	Elmar Platzgummer (IMS Nanofabrication)	Multi-Beam Mask Writer MBMW-101 for the 7 nm node, and beyond	42
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	8:40 – 9:05 PM	Martin Burkhardt (IBM)	Prospect of low-k1 Lithography in EUV	51
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Schedule of Presentations
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	8:50 – 9:15 AM	John Fourkas (Univ. of Maryland)	Progress Report on Photoresist Development for Multicolor Lithography	57
	9:15 – 9:40 AM	Nicole Lindermann (Nanoscribe GmbH)	3D Printing for Photonics Applications	58
	9:40 - 10:05 AM	Andres Torres (Mentor Graphics)	Reducing error placement sensitivity to guiding pattern distortions in cylinder forming DSA by optimizing grapho-epitaxy guiding templates.	59
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Session 8	10:35 – 11:00 AM	Uwe D. Zeitner (Fraunhofer-Institut für Angewandte Optik und Feinmechanik)	Alternative lithographic technologies for micro- and nano-optical applications	62
	11:00 – 11:25 AM	Britt Turkot (Intel)	To be announced	64
	11:25 – 11:50 AM	Dan Meisburger (Tec-Start Consulting)	The Maskless Lithography Revolution in PCB Production	65
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	12:15 – 12:40 PM	Hiroki Nakagawa (JSR)	Novel Spin-on Hard Masks Materials for 5nm Node and Beyond	68
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Schedule of Presentations **Wednesday, November 9, 2016**				
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	2:55 – 3:25 PM	Christopher Ober (Cornell Univ. / JSR)	EUV metal oxide photoresists: Finding common features between systems	73
	3:25 – 3:50 PM	Eric Hendrickx (imec)	Accurate modeling of EUV mask 3D effects and possible mitigations	74
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	6:30 – 9:00	**Banquet**		

Schedule of Presentations
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	8:50 – 9:15 AM	Patrick Shiavone (Aselta)	Why we should escape 1D-centric e-beam lithography flow	79
	9:15 – 9:40 AM	Leo Pang (D2S, Inc.)	GPU Accelerated Model-based Mask Data Preparation and Other Computational Applications in Semiconductor Manufacturing	80
	9:40 - 10:05 AM	Ravi Kanjolia (EMD Performance Materials)	Atomic Layer Deposition Materials: Key Enablers for New Processes	81
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	11:00 – 11:25 AM	Thomas Cecil (Synopsys)	Model Based Assist Features	85
	11:25 – 11:50 AM	Hakaru Mizoguchi (Gigaphoton)	To be announced	86
	11:50 – 12:15 PM	Eric Bouche (Ultratech)	Wafer shape process control in Foundry Lithography	87
	12:15 – 12:40 PM	Pieter Kruit (Delft / MAPPER)	From dose statistics to line edge roughness	88
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	2:05 – 2:30 PM	Naoya Hayashi (DNP)	To be announced	91
	2:30 – 2:55 PM	Alex Liddle (NIST)	Defectivity in Self-Assembled Structures	92
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Session 12	3:25 – 3:50 PM	Shigeki Nojima (Toshiba)	Machine learning for DFM applications	93
	3:50 – 4:15 PM	Hamed Sadeghian (TNO)	To be announced	94
	4:15 – 4:40 PM	Laurent Pain (CEA – Leti)	Latest results of MAPPER technology toward its industrialization ramp up	95
	4:40 – 5:00 PM	Martha Sanchez	Closing Remarks and Announcements	
	5:00 PM	End Session and Conference		

Poster Papers

Monday, November 7, 5:00 – 7:00 PM
Tuesday, November 8, 5:00 – 7:00 PM

Session 1

Presentation Schedule for
Monday, November 7, 2016

Session Chair
Martha Sanchez

	Time	Presenter	Title
Session 1	8:00 – 8:25 AM	Vivek Singh Martha Sanchez	Welcome
	8:25 – 9:15 AM	Bill Arnold (ASML) ***Keynote Speaker***	EUV Lithography: Current Status and Future Prospects
	9:15 – 9:40 AM	Greg Rechtsteiner (Cymer)	EUV Lithography: Current Status and Future Prospects
	9:40 – 10:05 AM	Eric Hendrickx	EUV insertion possibilities for N7 and N5 technology nodes
	10:05 – 10:35 AM	BREAK	

EUV Lithography: Current Status and Future Prospects

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ABSTRACT

With the advent of 7nm logic and 16nm DRAM, EUV lithography will be inserted for critical levels which otherwise must be defined with inefficient and increasingly uneconomic multi-patterning technology. EUVL has been developed to achieve substantially finer resolution than is available with 193nm immersion lithography in order to support shrinking design rules for CMOS manufacturing.

New manufacturing processes in as fundamental a role as lithography must meet many requirements such as strict variability control, productivity, and cleanliness. As a result, much focus has been brought to optics and mechatronics development, EUV source power improvement, increased tool availability, and the development of an innovative pellicle system [1].

In addition, a roadmap for the future is needed to ensure the further success of nanoelectronics manufacturing. A high numerical aperture scanner is studied for possible introduction for manufacturing in the next decade [2].

Keywords: EUVL, Overlay, Source Power, Pellicle, High Numerical Aperture

References:
[1] Alberto Pirati, et al, "EUV Lithography performance for manufacturing: status and outlook", *Proceeding of SPIE, Vol*. 9776, 2016
[2] Jan van Schoot, et al, "EUV high-NA scanner and mask optimization for sub-8nm resolution", *Proceedings of SPIE, Vol. 9776, 2016*

Effects of DUV light source tunable bandwidth on imaging performance

Greg Rechtsteiner[a], Paolo Alagna[b], Will Conley[a], Jason Shieh[c], Simon Hsieh[d], Tsann-Bim Chiou[c], Stephen Hsu[e]

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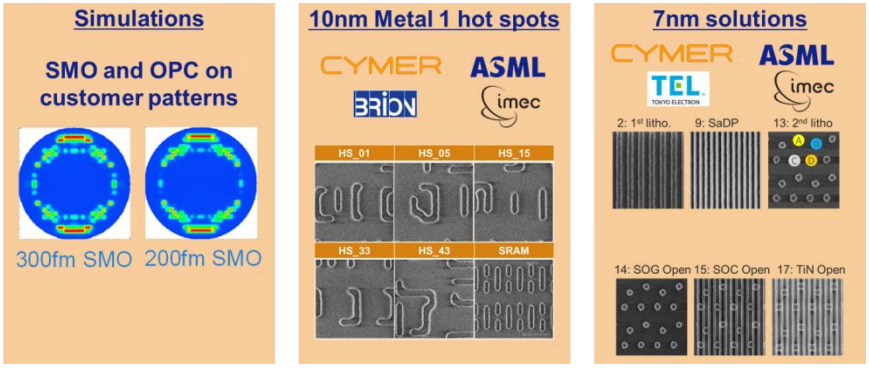
The performance requirements of advanced semiconductor technology nodes necessitate the use of complex processing methods that push patterning beyond the physical limits of DUV immersion lithography (ArFi). Specifically, aggressive process window (PW) and yield specifications put tight requirements on scanner imaging performance. As demonstrated by recent studies [1-4], a significant improvement to multiple patterning solutions can be achieved by leveraging light source capabilities.

This study will focus on the increase in image contrast that 200 fm light source E95 bandwidth enables on Self-Aligned Double Patterning (SADP) features. The impact of 200 fm E95 bandwidth on the CD and Edge Placement Error (EPE) performance of core (grating) and block features will be assessed using an imec 7 nm process node test vehicle.

The on wafer experimental results will be compared with simulations on the increase in image contrast that Source Mask Optimization (SMO) and OPC models deliver when using 200 fm light source E95 bandwidth. Using multiple patterning layouts that are aligned with projected 7 and 5 nm process node ground rules, improvements in Exposure Latitude (EL), Critical Dimension (CD) and Mask Error Enhancement Factor (MEEF) performance will be assessed when SMO and OPC are optimized for 200 fm light source bandwidth and compared with the standard 300 fm bandwidth.



[1] P. Alagna et al., “Optimum ArFi laser bandwidth for 10nm node logic imaging performance”, Proc. SPIE 9426, Optical Microlithography XXVIII, 942609 (2015).

[2] P. Alagna et al., “Lower bandwidth and its impact on the patterning performance”, Proc. SPIE 9780, Optical Microlithography XXIX, 978008 (2016).

[3] W. Conley et al., “Impact of bandwidth on contrast sensitive structures for low k1 lithography”, Proc. SPIE 9426, Optical Microlithography XXVIII, 942607 (2015).

[4] W. Conley et al., “Impact of bandwidth variation on OPC model accuracy”, Proc. SPIE 9780, Optical Microlithography XXIX, 9780K (2016).

EUV insertion possibilities for N7 and N5 technology nodes

Christopher Wilson[a], Stephane LaRiviere[a], Bogumila Kutrzeba Kotowska[a], Danilo De Simone[a], Joost Bekaert[a], Jeroen Van de Kerkhove [a], Peter De Bisschop[a], Ming Mao[a], Geert Vandenberghe[a], Kurt Ronse[a], Ryoung-han Kim [a], Eric Hendrickx[a]

[a] imec

EUV lithography has seen rapid progress over the last 2 years. ASML NXE:3300 production tools have been installed at the main chipmakers, and are being tested for pilot production. Most importantly, the rapid improvement in EUV source power has restored credibility to the source roadmap and is a key enabler of the technology. Overall the technology is at the doorstep of production. In this presentation we will review the status of the EUV resists, masks, and scanner, and how these improvements come together in foundry-equivalent N7 and N5 BEOL process modules that are developed at imec to demonstrate the readiness of EUV technology.

We have used the ASML NXE 3300 to fabricate foundry-equivalent N7 product like wafers with both trench and via patterns. Here, compared to 193i, EUV offers the possibility of a single print for advanced nodes. For comparison, we have also developed and tested 193i lithography based flows using multiple litho etch (LE) and doubling pattering (SADP+Keep) to reach sub resolution pitch. The EUV single print flow showed better CDU but slightly worse LWR when compared to the 193i lithography based flows. In either case CDU and LWR can lead to open or bridging. Overlay, litho-etch bias uniformity and line end pull back were key issues to solve in developing these 193i lithography based flows. Greater corner rounding was observed in both the litho etch and litho-etch and double pattering flows when compared to the EUV single print flow. This resulted in clearly better patterning fidelity in the EUV single print flow compared to the 193i lithography based solutions.

Towards the foundry-equivalent N5 technology nodes, a patterning exercise is ongoing for a new imec BEOL process module. Here the metal patterning is done by combining an SAQP grating, fabricated by 193i, and a block layer printed using EUV lithography. We review 2D imaging results from the N5 like block layer for metal patterning. This includes using a metal containing resist, and includes etch transfer with a variety of chemistries. We show the different patterning options, and present experimental results obtained from imec's BEOL N5 EUV platform, with focus on litho performance and process integration.

Session 2

Presentation Schedule for
Monday, November 7, 2016

Session Chairs
Carlos Fonseca
Patrick Naulleau

	Time	Presenter	Title
Session 2	10:35 – 11:00 AM	Ankit Vora (IBM Research Almaden)	Topcoat-free Strategies for Orientation Control of All-organic High-χ Block Copolymers
	11:00 – 11:25 AM	Michael Thompson (Cornell Univ. / JSR)	Kinetics of BCP segregation and DSA alignment during millisecond spike annealing
	11:25 – 11:50 AM	Nihar Monhanty (TEL Technology Center)	Patterning when variability rules the roost
	11:50 – 12:15 PM	Hiroshi Matsumoto (NuFlare Technology)	Multi-beam mask writer MBM-1000
	12:15 – 12:40 PM	Keita Sakai (Canon)	A Review of Nanoimprint Wafer and Mask Tool Progress and Status for High Volume Semiconductor Manufacturing
	12:40 AM	End Session	

Topcoat-free Strategies for Orientation Control of All-organic High-χ Block Copolymers

Ankit Vora[1]*, Joy Y. Cheng[1], Melia Tjio[1], Noel Arellano[1], Kristin Schmidt[1], Anindarupa Chunder[1], Teddie Magbitang[1], Elizabeth Lofano[1], Hsinyu Tsai[2], Hiroyuki Miyazoe[2], and Daniel P. Sanders[1]

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[2] *IBM Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY, 10598*

Directed self-assembly (DSA) of block copolymers (BCP) is a promising candidate for extending the patterning capability of conventional lithography. While PS-b-PMMA is the most widely used block copolymer for DSA, the minimum half-pitch of this BCP is limited to ~10nm because of the low interaction parameter (χ) between PS and PMMA blocks. Higher-χ BCPs (e.g. PS-b-PEO, PS-b-P2VP, PS-b-PTMSS, etc.) capable of smaller natural period, the *L*o, are expected to be necessary for patterning for sub-10nm IC (integrated circuit) devices. But due to the increased mismatch in the surface energies of the two blocks of high-χ BCP, only the lower surface energy block is present at the polymer-air interface, rendering the thin-film undesirable for lithographic applications. Previously, we had discussed a formulation-based approach in which a surface active polymer (SAP) was added as an additive to enable perpendicular orientation control of polycarbonate-containing high-χ BCPs (Figure 1) using a coat and a short thermal annealing step on neutral underlayer modified substrates (Gen. 1 BCP).

To further improve the robustness of the BCP material and make it more integration-friendly for DSA processing, an additive free high-χ BCP platform (Gen. 2 BCP, Figure 2) that forms vertically oriented features upon thermal annealing on a wide range on underlayer compositions was developed. In this talk, the development and performance of Gen 2. BCP platform will be discussed. Specifically, the thin-film characterization by AFM and GISAXS to confirm perpendicular orientation, and the effect of thermal annealing conditions and underlayer composition on self-assembly behavior of the lamellae forming BCPs will be detailed. Next, the DSA, etch, and pattern transfer of the Gen. 2 BCP will be highlighted. Finally, the advantages and the limitations of Gen. 1 and Gen. 2 high- χ BCPs will be compared with respect to sub-20 nm pitch patterning.

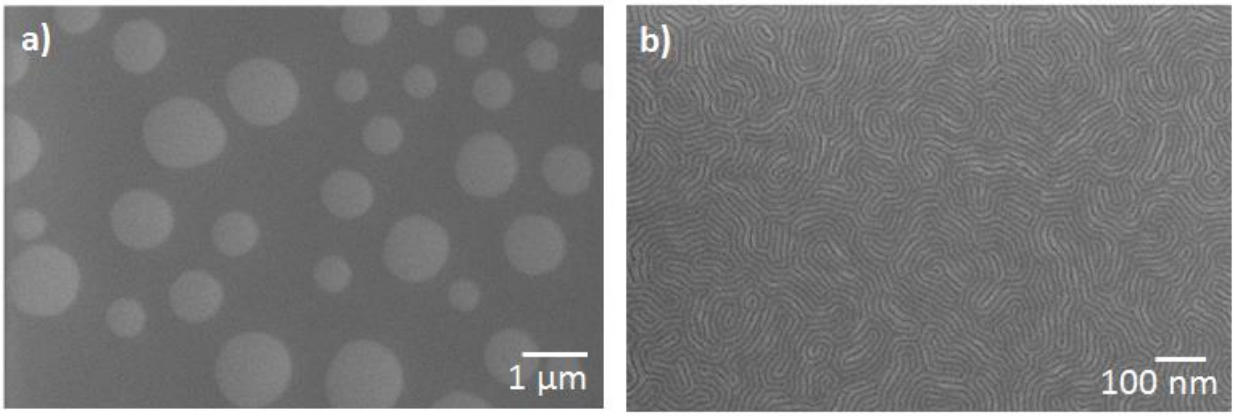

Figure 1. Thin film self-assembly of 19.5 nm pitch polystyrene-*b*-polycarbonate BCP (Gen. 1 BCP) on neutral underlayer modified substrate, a) without SAP additive and b) with 3 wt. % SAP additive. BCP films were annealed at 170 °C for 5 minutes.

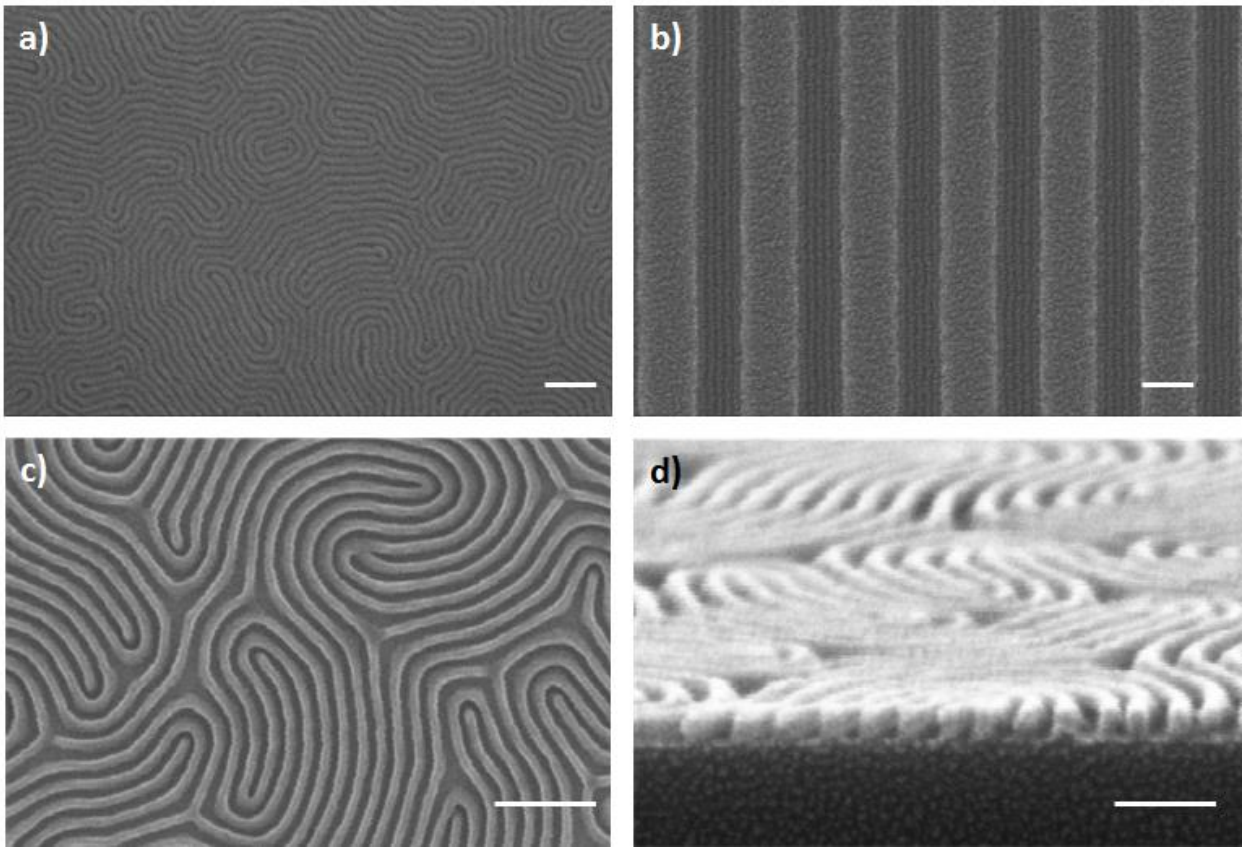

Figure 2. Vertically oriented features for 18.3 nm pitch Gen. 2 BCP upon thermal annealing at 170 °C for 5 minutes. a) fingerprint patterns on neutral underlayer modified substrate, b) 5X graphoepitaxy DSA on prepattern prepared by 193 nm interference lithography, c) Top-down and d) Cross-section SEM images of ~9 nm HP BCP fingerprint patterns after removing one of the blocks of the BCP. Scale bar = 100 μm.

Kinetics of BCP segregation and DSA alignment during millisecond spike annealing

Michael O. Thompson, Alan G. Jacobs, Jing Jiang, Christopher K. Ober,
Materials Science and Engineering, Cornell University, Bard Hall, Ithaca, NY 14853

Directed Self Assembly (DSA) of block copolymers (BCP) remains a key potential technology for patterning at sub-7 nm nodes. Achieving requisite alignment precision and reliability, while addressing line edge roughness and etch selectivity, requires understanding of fundamental segregation processes and exploration of alternate processing. In this work, we used millisecond thermal annealing, induced by laser spike annealing (LSA), to map the kinetics of BCP phase segregation and understand the role of this annealing on the eventual development of alignment order during graphoepitaxially directed DSA.

LSA annealing near or above the ODT (order-disorder transformation temperature) can dramatically improve the fidelity of DSA alignment. The early stage segregation behavior, which impacts this final structure, were explored using a later-gradient LSA method with micro-beam grazing incidence small angle X-ray scattering. Ordering and disordering kinetics of cylinder forming PS-b-PMMA were determined for annealing temperatures up to 550 °C and dwells ranging from 250 μs to 10 ms. Both ordering and disordering kinetics were independently monitored. From initially microphase segregated films, disordering began near the equilibrium ODT temperature for dwell times above 10 ms. For shorter times, this disorder is kinetically delayed increasing by over 70°C for 250 μs with asymptotic behavior for times below 50 μs. The onset of ordering from initially disordered films was similarly kinetically limited. For anneals to temperatures well above the ODT, films become fully disordered and the final segregation behavior is determined solely by the thermal quench rate through the ODT and to the glass transition temperature. This results in a history independent final state that forms the initial configuration for further thermal annealing. This kinetic behavior can be represented on an effective Tg and ODT temperature phase map as a function of the heating timescale (figure 1). Thermal processing of the BCP to retain or intentionally modify the initial state can thus be independently managed with accelerating kinetics for other chemical or structural alignment processes at the extreme temperatures.

Graphoepitaxial DSA is enabled by dramatic increases in polymer chain mobility at these temperatures. Optimal DSA alignment was observed with LSA anneals in the 5-20 ms range, still well before polymer decomposition can occur. Effects of laser power, dwell time, underlayer and graphoepitaxy were examined with long range order and alignment achieved with 20 ms laser annealing.

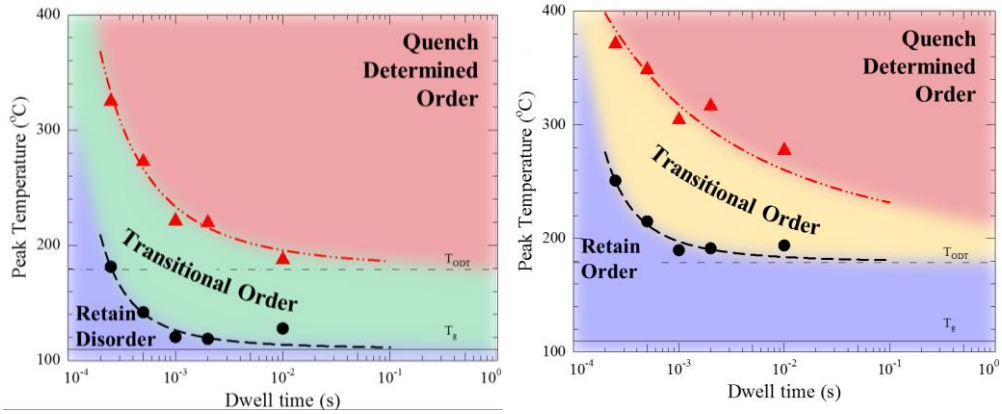

Figure 1: Kinetic phase map for segregation behavior as a function of annealing dwell for initially disordered films (left) and initially ordered films (right).

Patterning when variability rules the roost

Nihar Mohanty, Jeffrey Smith, Anton deVilliers, Hidetami Yaegashi, Richard Farrell, Ben Rathsack, Carlos Fonseca, Akiteru Ko, Steven Scheer, Peter Biolsi

TEL Technology Center America, LLC. NanoFab South, Ste. 214, Albany, NY 12202

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Ever since the Moore's law was first coined, the semiconductor industry has diligently followed the path where making devices smaller resulted in lower price per transistor, higher performance gain and more profits. While in the beginning lithographic advances played a major role in enabling the regular cadence of areal shrinkage, in the recent past, materials and smart integration have been instrumental in assisting lithography for continued scaling. As the industry marches on to the 5nm node and beyond, scaling has slowed down, with all major IDMs & foundries predicting a 3-4 year cadence for scaling. A major reason for this slowdown is not the technical challenge of making features smaller, but effective control of the variation that creeps into the fabrication process. That variability manifests itself as edge placement error (EPE) which has a direct impact on wafer yield (Figure – 1). Resolving EPE concerns necessitates an integrated approach between unit process, materials development, process integration and design.

$$EPE_{random} = \sqrt{\left(\frac{\sigma_{CD1}}{2}\right)^2 + \left(\frac{\sigma_{CD2}}{2}\right)^2 + \left(\frac{\sigma_{CD3}}{2}\right)^2 + \left(\frac{\sigma_{CD4}}{2}\right)^2 + (\sigma_{OL1})^2 + (\sigma_{OL2})^2 + (\sigma_{OL3})^2 + (\sigma_{OL4})^2}$$

CD variability includes CDU, LCDU & LER/LWR

Overlay is dominant for EPE

Figure 1: Both CD variability and overlay form major contributors to the EPE. EPE is one of the most critical variability issues faced by the semiconductor industry today.

In this paper we will provide a brief overview of our current and upcoming EPE and overlay improvement techniques with special emphasis on self-alignment & self-healing based approaches. The key enabler for most self-alignment based approaches is the ability to trade-off the un-manageable overlay requirement with that of a more manageable etch selectivity requirement (Figure 2). By

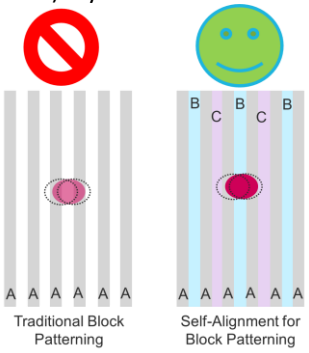


Figure 2: Comparison of traditional vs. self-alignment based patterning showing how by a multi-color material integration, the overlay variation becomes in-consequential thereby reducing the over all EPE. The black lines labelled A are spacer-formed-lines with space being the trench and red ellipse is the block pattern. As evident from the figure, any overlay variation could cause the adjacent trench to get un-intentionally blocked. To enable self-alignment we fill every other trench with a different sacrificial material labeleld B and C. By having high selectivity between A, B and C, self-alignment of blocks can be achieved. This precludes any variation from block pattern overlay.

appropriate choice of different mask and stack materials this etch selectivity challenge can be made trivial. We will present several case studies for both logic & memory, which would cover some of the most critical layer patterning, where we will demonstrate how the implementation of self-alignment & self-healing alleviates key variability concerns. Further, we will also present on the design advantage that the new approaches provide based on common standard cell designs and their potential for simplifying or shortening the design technology co-optimization (DTCO) process during development lifecycle of a technology node. We will conclude the talk with our view on the future direction for industry on patterning & design as a major tool maker.

Multi-beam mask writer MBM-1000

Hiroshi Matsumoto, Hiroshi Yamashita, Kenji Ohtoshi, Hirokazu Yamada
NuFlare Technology, Inc

Progress of shrinkage of semiconductor devices has slowed down, but strong motivation for further shrinkage persists. ArF immersion lithography has been extended by introducing multiple patterning and aggressive OPC. Continuous efforts on EUV lithography accomplished increase of light source enabling pilot fabrication. Evolution of lithography and shrinkage of device pause challenges for mask writers in terms of increase of shot count, number of photomasks and exposure dose as well as more and stringent writing accuracy.

Single variable shaped beam (S-VSB) writer has been used for advanced photomasks in recent decades, but big leap in shot count likely demanded by aggressive OPC or EUV lithography will trigger switch to multi-beam writers. Aiming application to N5, we will launch MBM-1000, our 1st product of multi-beam mask writer based on system with blanking aperture array (BAA).

In this paper, we will introduce features of our MBM-1000 with comparison to S-VSB writers, to discuss suitable application field in lithography for MBM-1000 and S-VSB writers. We will also report results of patterning test with MBM-1000 alpha tool.

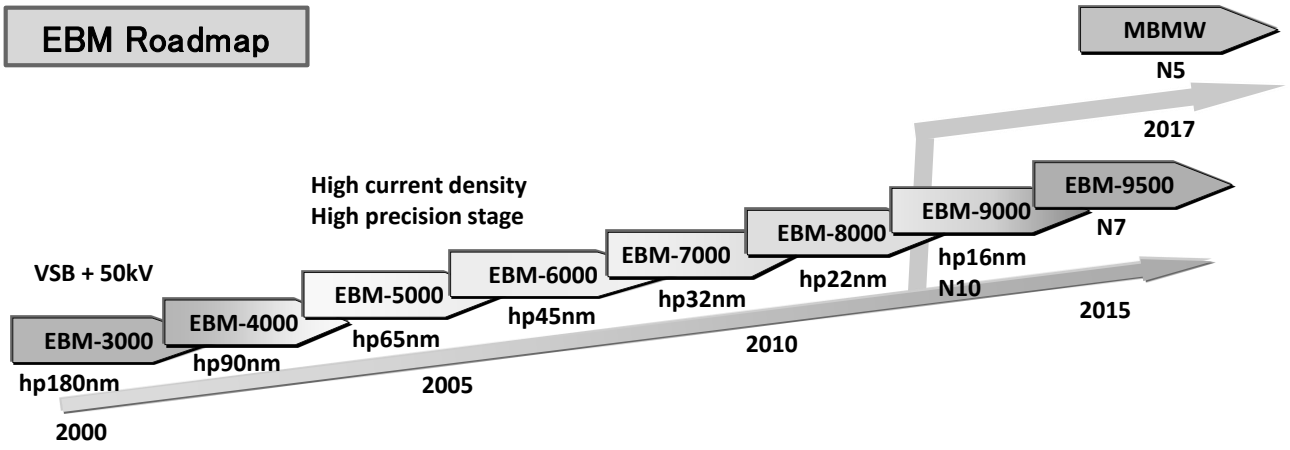


Figure: History of mask writers in NuFlare Technology Inc.

A Review of Nanoimprint Wafer and Mask Tool Progress and Status for High Volume Semiconductor Manufacturing

Keita Sakai
Canon Inc., 20-2, Kiyohara-Kogyodanchi, Utsunomiya-shi, Tochigi 321-3292 Japan

Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.

There are many criteria that determine whether a particular technology is ready for wafer manufacturing. Included on the list are overlay, throughput and defectivity. The most demanding devices now require overlay of better than 4nm, 3 sigma. Throughput for an imprint tool is generally targeted at 80 wafers per hour. Defectivity and mask life play a significant role relative to meeting the cost of ownership (CoO) requirements in the production of semiconductor devices. Hard particles on a wafer or mask create the possibility of inducing a permanent defect on the mask that can impact device yield and mask life. By using material methods to reduce particle shedding and by introducing an air curtain system, the lifetime of both the master mask and the replica mask can be extended. In this presentation, we review the latest results that demonstrate a path towards high volume manufacturing of advanced devices.

On the mask side, a new replication tool, the FPA-1100 NR2 is introduced. Mask replication is required for nanoimprint lithography (NIL), and criteria that are crucial to the success of a replication platform include both particle control, resolution and image placement accuracy. In this presentation we also discuss the progress made in both feature resolution and in meeting the image placement specification for replica masks.

*Jet and Flash Imprint Lithography and J-FIL are trademarks of Molecular Imprints Inc.

Session 3

Presentation Schedule for
Monday, November 7, 2016

Session Chairs
Alan Brodie
Alex Liddle

	Time	Presenter	Title
Session 3	7:00 – 7:25 PM	Qi-Huo Wei (Kent State / Liquid Crystal Inst.)	Projection Photopatterning Molecular Orientations in Liquid Crystals by Using Novel Plasmonic Metamasks
	7:25 – 7:50 PM	Hiroshi Fukuda (Hitachi High Technology)	Electron beam-based metrology and inspection, overcoming the limitation of scaling, variability, and productivity
	7:50 – 8:15 PM	Mike Rieger (Synopsys)	Patterning for advanced integrated devices
	8:15 – 8:40 PM	Vito Dai (Motivo)	Physical Design Characterization and Optimization with Graph-based Search, Advanced Analytics and Machine Learning
	8:40 – 9:05 PM	Tatsuhiko Higashiki (Toshiba)	Progress and challenges in Imprint Lithography
	9:05 – 9:30 PM	Bob Socha (ASML)	Alignment mark optimization for improved on-product overlay (OPO) performance
	9:30 PM	End Session	

Projection Photopatterning Molecular Orientations in Liquid Crystals by Using Novel Plasmonic Metamasks

Qi--Huo Wei

Liquid Crystal Institute, Kent State University, Kent, OH44242, USA *qwei@kent.edu*

The manufacturing of liquid crystal (LC) display panels has greatly facilitated the technology developments for aligning LC molecules into uniform orientations at substrate surfaces. However, many emerging applications of LC materials such as Pancharatnam lens, programmable origami and directed colloidal assembly rely on spatially non--uniform molecular alignments. To meet this high demand, we propose and develop a new projection photoalignment technique based on nanostructured plasmonic metamasks (PMMs). The PMMs are made of two dimensional arrays of rectangular nano--holes in thin aluminum films. When illuminated by non--polarized white light, the PMMs can generate spatially non-uniform polarization patterns. By exposing photoactive materials with light transmitted through the PMMs, complex molecular orientation patterns encoded in the PMMs can be induced in the photoactive materials and then transferred into bulk LCs. We show that this technique enables the control of two-- and three-dimensional LC molecular orientation with unprecedentedly high spatial resolution and with practically any designer complexity. This mask--based patterning technique features high throughput, repeatability, low cost and scalability for large volume liquid crystal device manufacturing.

This plasmonic photopatterning technique enables new capabilities. I will show two examples: one is related to a new scheme to generating and reconfiguring disclination networks in nematic LCs, the other is related to a versatile approach to generate electrokinetic flows in LCs by using predesigned molecular orientations. These two capabilities make the LCs an attractive medium for colloidal assembly and microfluidics device applications.

Short Bio:

Dr. Qi--Huo Wei is currently an associate professor in the Liquid Crystal Institute and Department of Chemical Physics at Kent State University. He received his PhD in Physics from Nanjing University in China. Before Joining Kent State University, he worked in multiple places, including the Biodesign Institute at Arizona State University and University of California at Los Angeles. He is a recipient of NSF CAREER award. The research of his group at the Liquid Crystal Institute is multidisciplinary, covering soft and active matter, plasmonic nanophotonics, micro/nanomanufacturing.

Electron beam-based metrology and inspection, overcoming the limitation of scaling, variability, and productivity

H. Fukuda and Y. Momonoi
Hitachi High-Technologies Corporation, Tokyo, Japan

Continuously shrinking design rule into single-digit nodes and introduction of new device materials/structures require complex process steps and tight process control in etching, deposition, and CMP as well as in lithography. The e-beam based metrology and inspection have widely been used in high-volume-manufacturing (HVM) of semiconductor devices. While their sub-nanometer precision provides infrastructures as the standard ruler in HVM environment today, their high-resolution direct visualization of devices is indispensible for quick process diagnostics in ramping-up phase, such as material/structure and process window analyses.

In 10-nm node and beyond, the local changes in pattern features due to systematic/stochastic variation are becoming major contributor in edge-placement-error (EPE) together with the conventional CD variation and overlay error. Also, introduction both of multiple patterning and of EUV lithography requires tighter process control and management of huge number of hot-spots in real circuit features, which limit the effective process windows. E-beam technology is suitable for detecting such local changes, while these requirements pose challenges in throughput while keeping necessary resolution and precision, because they require huge number of measurement to guarantee statistical reliability. This is a kind of paradigm shift in semiconductor pattern metrology and inspection, which is now the measurement of variation and exploration of occurrences/locations where variation is out of tolerance.

Another challenge includes ever complicated three-dimensional structures such as 3D-NAND, various self-aligned/self-limited structures, and GAA-NW transistor. Slight differences in the nature of scattered electron have to be detected and analyzed. This requires a close look at physics of beam-matter interaction and collaboration between metrology and device development.

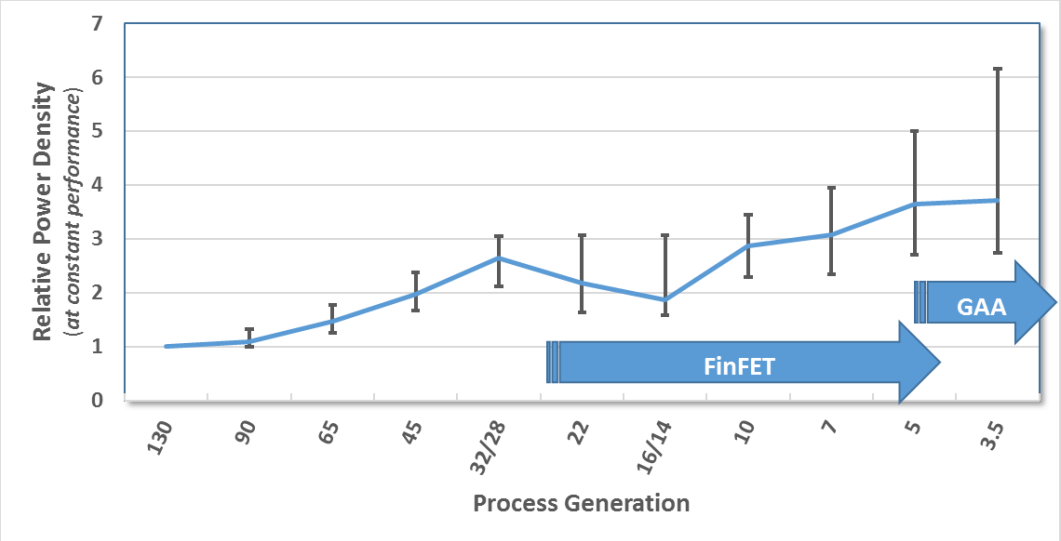
Finally, the precision of metrology tool fleet have to be kept within a sub-nm range to serve as an infrastructure to support HVM.

In summary, we believe that e-beam metrology and inspection is playing more and more important role in 10-nm node and beyond for enhancing process ramp-up speed and for achieving high yield in HVM. This talk will highlight and discuss some of the challenges and prospects of e-beam techniques to tackle/overcome the above challenges.

Patterning for advanced integrated devices

Mike Rieger, Victor Moroz
Synopsys

With known patterning and device options CMOS transistor density scaling likely can continue, consistent with Moore's Law, for at least two generations beyond the 7nm node. From a chip-design perspective, a growing challenge will be dealing with ever-increasing power density (watts/area), something that became a key concern two decades ago when voltage scaling began to flatten. Without voltage scaling, power efficiency per device improves more slowly than device density. FinFETs provided a step function improvement in power-performance but, with further scaling, power density is again rising. Another step advancement, the gate-all-around (GAA) or "nanowire" FET, is just around the corner; however, unless switching voltages can be reduced sufficiently, power density will continue to be a concern.



There is headroom between the actual voltages used in CMOS ICs and the voltage floor set by the fundamental electrostatics of MOSFET technology. This excess voltage margin is needed to deal with variation in device electrical characteristics. Dynamic power, $\sim FCV^2$, is proportional to the square of the switching voltage and significant improvements in power efficiency can be achieved by reducing threshold-voltage variation to enable lower switching voltage. Advanced CMOS electrical characteristics are becoming increasingly sensitive to geometric variations, thus magnifying the electrical effects of patterning imperfections. The impact of lithography properties and patterning choices on IC power and performance will be explored in this talk.

Physical Design Characterization and Optimization with Graph-based Search, Advanced Analytics and Machine Learning

Vito Dai, Edward Kah Ching Teoh, Ji Xu, Bharath Rangarajan
Motivo, Inc.

Integrated circuit (IC) manufacturing yield is the result of complex high dimensional layout configurations (geometrical patterns) interacting with process parameters, materials, tool settings, and actual random events. Characterization of yield-limiting layout configurations is of paramount importance to design and process simulation and to the understanding of physical defects and electrical failures of IC devices.

To analyze and quantify design variability, which are the source of the yield-limiting layout configurations, we present a method to systematically characterize the space of all possible configurations. All potential design variations are part of this space, and therefore, the coverage of this space by any given design layout can be computed. Coverage can be compared between designs, for example, test chip vs. product, or product A vs. product B to quantify key coverage differences. Furthermore, the configurations for which there is a lack of coverage can also be computed. These "missing" configurations are used to systematically drive data acquisition, resulting in complete characterization of the entire configuration space.

The configuration space is represented by a massive network graph, with nodes representing configurations, and multi-edges linking related configurations. Observational data for each configuration, such as simulation, metrology, defects and failure data can be further annotated onto each node. Graph search and machine learning algorithms are applied to the graph to identify and eliminate yield-limiting configurations. As a result, integrated circuit designs can be effectively optimized for manufacturing yield.

Progress and challenges in Imprint Lithography

Tatsuhiko Higashiki
(Toshiba)

Abstract not available at time of printing

Alignment mark optimization for improved on-product overlay (OPO) performance

Robert Socha[1], Boris Menchtchikov[1], Hielke Schoonewelle[2], Sudhar Raghunathan[1], Paul Tuffy[1], Patrick Tinnemans[2]

1. ASML Brion, 2. ASML Veldhoven

Wafer alignment is a critical function for on-product overlay performance. Wafer alignment marks in customer product stacks are impacted by processes which change the shape of the marks. If the change of the shape is asymmetrical, the wafer alignment error can increase, which will impact on product overlay performance. ASML has a created software simulator called D4C alignment which designs wafer alignment marks with minimal sensitivity to process variations while also having good detectability and measurement reproducibility. All of these aspects guarantees customers will have a wafer alignment mark which is optimized for overlay performance for given layers.

To test the ability of D4C alignment to improve alignment performance and reduce on-product overlay, experimental wafers from two wafer processes were created to deliberately introduce asymmetry into the alignment marks. The wafer processes with deliberate asymmetry are: etching into Si and CMP. Etching process can asymmetrically change side wall angle of the marks while Chemical Mechanical Planarization (CMP) process can deform top side of the alignment gratings (Figure 1).

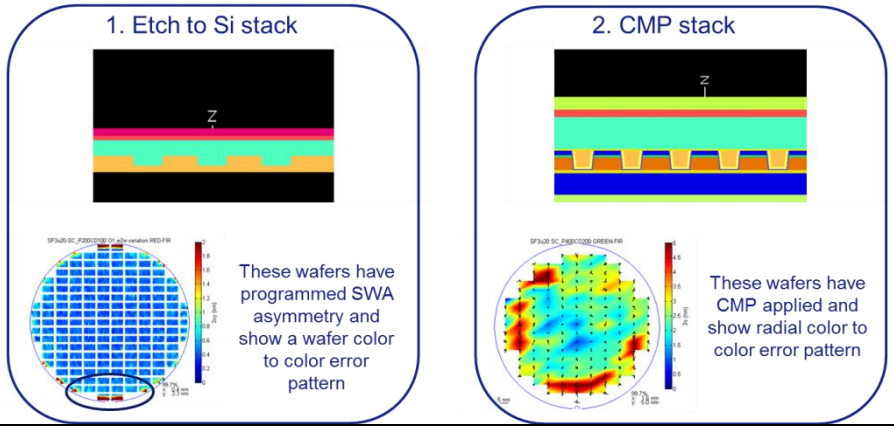


Figure 1. Test wafers with a pre-defined asymmetry from etch and from CMP were created to qualify asymmetry sensitivity prediction. Etch asymmetry (left) and CMP asymmetry (right) were deliberately created in the alignment marks.

The qualification has consisted of three phases:

1. Establish relation between asymmetry of a mark and SMASH alignment signal
2. Show that alignment performance influences measured overlay on YS
3. Show the simulation can predict YS overlay performance

In the presentation, essential results for each step will be presented. The mark asymmetry causes align position error. This error can be quantified by aligning the wafer with one wavelength (color) and by another wavelength (color). The color to color (C2C) align position deviation KPI (key performance indicator) is created by subtracting the alignment position of the two marks. Marks with lower C2C align position deviation KPI are less susceptible to asymmetry from the process. The D4C KPI reduces the color to color (C2C) align position rather than maximizing mark wafer quality (WQ) contrast. The D4C KPI of alignment mark sensitivity to asymmetry can be correlated to overlay performance measured on YieldStar (YS). In an experiment, many mark types with various segmentation were created to test the ability of the C2C align position deviation KPI to predict wafer to wafer (W2W) overlay error. In Figure 2, measurement results show marks with the lowest C2C measured align position KPI (green line) are least sensitive to process-variations; and, therefore, improve on-product overlay performance, YS W2W overlay error (blue bars). And the D4C color to color (C2C) KPI is a better predictor of overlay performance than mark wafer quality (WQ) contrast (brown line).

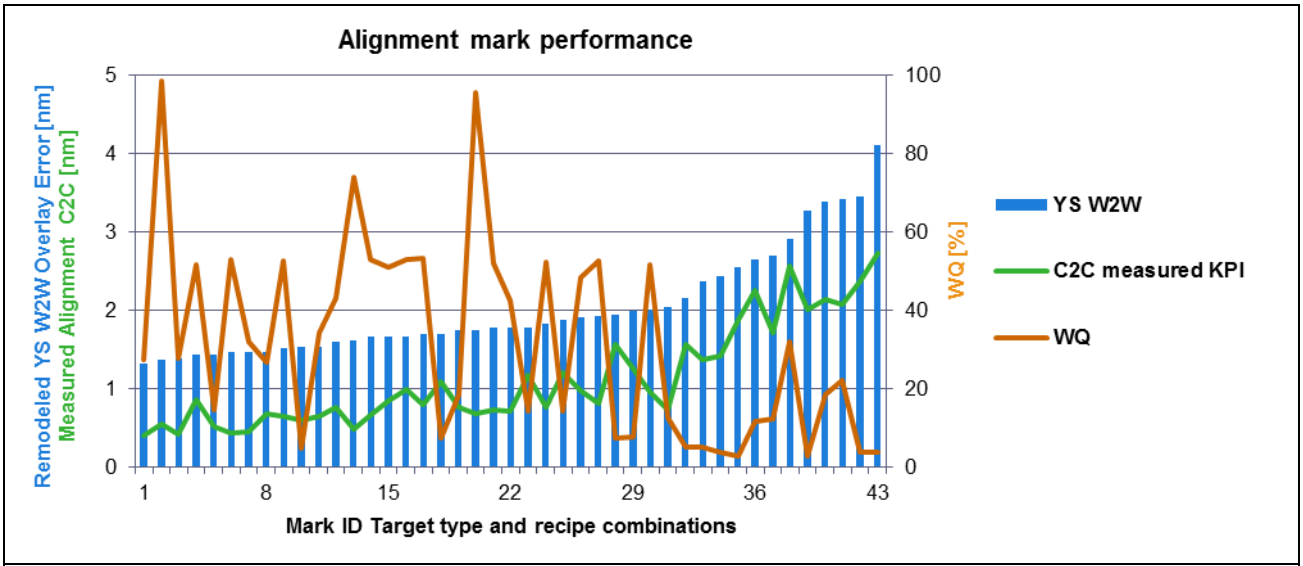


Figure 2. Comparison of two alignment KPI's (key performance indicator) to predict YieldStar (YS) measured wafer to wafer (W2W) overlay performance (blue bars). D4C color to color (C2C) KPI is a better predictor of overlay performance than mark wafer quality (WQ) contrast (brown line).

The results from this qualification show with computation from D4C-alignment it is possible to design alignment marks which are least sensitive to process variations, and, therefore, improve on-product overlay performance.

Session 4

Presentation Schedule for
Tuesday, November 8, 2016

Session Chairs
Chris Ober
Martin Burkhardt

	Time	Presenter	Title
Session 4	8:00 – 8:50 AM	Shinji Okazaki (Gigaphoton) ***Keynote Speaker***	Lithography: A key enabler for Moore's law scaling
	8:50 – 9:15 AM	Jean-Pierre Cloarec (Universite de Lyon)	Collective self-assembly of large sets of nanoparticles on nanopatterned functionalized substrates
	9:15 – 9:40 AM	Ben Bundy	
	9:40 – 10:05 AM	Puneet Gupta (UCLA)	Design-Technology_Co-Optimization Applications to EUV and DSA Process Technologies
	10:05 – 10:35 AM	BREAK	

Lithography: A key enabler for Moore's law scaling

Shinji Okazaki
Gigaphoton Inc.
400 Yokokura-Shinden, Oyama, Tochigi
323-8558 Japan

The development of ULSI devices has been stimulated by the miniaturization of the device feature size on a silicon chip. The development of optical lithography and electron beam lithography contributed a lot to this miniaturization. The roles of optical lithography and electron beam lithography are different. Optical lithography has been used as a main patterning tool for ULSI fabrication. On the other hand, electron beam lithography has been used as a mask fabrication tool. The former pursued higher resolution and the latter pursued higher throughput. The development history of these technologies will be reviewed and the future perspectives of these technologies will be discussed.
As the successor of optical lithography, EUV lithography has been intensively developed but the development speed was very slow. However, recent development results of EUV lithography show remarkable improvements. As a result, we will be able to expect the practical use of EUVL in industrial environments within several years. According to the improvements in light source power, various issues are also revealed. The future prospects of EUV lithography will also be discussed.

Collective self-assembly of large sets of nanoparticles on nanopatterned functionalized substrates

F. Palazon[1], S. Ansanay-Alex[1], P. Rojo-Roméo[1], C. Chevalier[1], T. Géhin[1], A. Bélarouci[1], E. Laurenceau[1], T. Le Mogne[2], D. Léonard[3], J-F. Bryche[4,5], G. Barbillon[4], B. Bartenlian[4], A. Olivero[5,6], M. Sarkar[5], M. Besbes[5], E. Maillart[6], J. Moreau[5], M. Canva[5] ,Y. Chevolot[1] & J.P. Cloarec[1]

1) Université de Lyon, Ecole Centrale de Lyon, Institut des Nanotechnologies de Lyon, CNRS UMR 5270
2) Ecole Centrale de Lyon, Laboratoire de Tribologie et Dynamique des Systèmes, UMR CNRS 5513
3) Institut des Sciences Analytiques, CNRS UMR 5280, Villeurbanne France
4) Institut d'Electronique Fondamentale, CNRS UMR 8622, Orsay, France
5) Laboratoire Charles Fabry de l'Institut d'Optique, CNRS UMR 8501 Palaiseau, France
6) Horiba Jobin Yvon SAS, Palaiseau, France

Material science allows to synthesize a large diversity of nano-objects, through bottom-up processes; these nano-objects can exhibit various properties to be potentially applied in photonics, electronics, chemistry and biology. DNA origami, multifunctional nanoparticles, nanowire, carbon nanotubes are examples of such nano-objects.

Embedding these nano-objects into devices (e.g. nanotransistor, nanophotonic structure) is envisioned for elaborating new ultrasensitive sensors or new information processing components. However, even if these nano-objects exhibit interesting properties, they can be useful only if they are located and robustly anchored on final devices, with a nanometric precision. Moreover, the method used for addressing and anchoring the nano-objects should be compatible with mass production processes.

We explored how self-assembly may be used for addressing bottom-up synthesized nanoparticles on simple gold nanostructures elaborated with top-down electron beam lithography.

Silicon dioxide substrates covered with a matrix of 50x300 nm gold nanostructures were chemically functionalized in a one-pot reaction, using two different coupling agents, namely a mixture of silane and alkylthiol. Resulting surfaces were characterized using TOF-SIMS and XPS imaging. Characterizations show that during this one-pot reaction, silane molecules specifically bound to SiO_2 zones, while thiols specifically bound to gold nanostructures. Nanoparticles exhibiting a strong affinity for the functionalized gold nanostructures were left to self-organize on the surface. Scanning Electron Microscopy images show that nanoparticles do not physisorb on SiO_2, while they are spontaneously captured on gold nanostructures.

We will show how this approach combining top-down lithography and bottom-up self-assembly is envisioned to implement ultrasensitive nanobiosensors.

Reference : Palazon, F., Rojo-Romeo, P., Chevalier, C., Géhin, T., Belarouci, A., Cornillon, A., ... Chevolot Y. & Cloarec, J. P. (2015). Nanoparticles selectively immobilized onto large arrays of gold micro and nanostructures through surface chemical functionalizations. *Journal of colloid and interface science*, 447, 152-158.

HVM metrology for 5 nm

Ben Bundy

SEMATECH

Abstract not available at time of printing

Design-Technology_Co-Optimization Applications to EUV and DSA Process Technologies

Puneet Gupta
UCLA

This work will focus first with a discussion on the impact of design layout on EUV mask yield. We propose a "critical density" measure to assess mask yield in presence of blank defects when pattern-shift is employed as a defect avoidance technique. We show that, surprisingly, regular layouts are likely to be layouts most susceptible to blank defects. In the second half of the talk we describe a novel design-technology path-finding framework for DSA. The framework optimally evaluates a DSA-based technology for vias/contacts, where an arbitrary lithography technique is used to print the guiding templates, possibly using several masks/exposures steps and provides a design friendliness metric.

Session 5

Presentation Schedule for
Tuesday, November 8, 2016

Session Chairs
Donis Flagello
Bob Socha

	Time	Presenter	Title
Session 5	10:35 – 11:00 AM	Bernd Geh (Zeiss)	EUV and flexible illumination for 5 nm Lithography and beyond
	11:00 – 11:25 AM	Naoya Hayashi (DNP)	EUV Masks
	11:25 – 11:50 AM	Elmar Platzgummer (IMS Nanofabrication)	Multi-Beam Mask Writer MBMW-101 for the 7 nm node, and beyond
	11:50 – 12:15 PM	Marie Krysak (Intel)	Stochastic and Non-Stochastic CD variations in Next Generation Lithography
	12:15 – 12:40 PM	Deirdre Olynick (LBNL)	Elements for EUV Electronic Resist Amplification
	12:40 PM	End Session	

EUV and flexible illumination for 5 nm Lithography and beyond

Bernd Geh[*], Jörg Zimmermann, Paul Gräupner, Ralf Gehrke, Alexander Winkler, Stephen Hsu[+], Christoph Hennerkes[+]
Carl Zeiss SMT GmbH (Germany)
+ ASML Brion (United States)
* Carl Zeiss / ASML-TDC (United States)

As the industry is moving towards the 2020s the continued shrink is pushing technical and economical limits. The complexity of patterning solutions explode as we strive to remain on track with technology roadmaps. As shrinking continues, conventional optical Lithography requires more and more complicated landscapes of overlay and alignment strategies as well as many additional exposure and processing steps. Single exposure EUV lithography has now been widely accepted as an enabler for continued logic device scaling at affordable cost.

Aggressive design rules for the 5 nm node translate into k1 factors below 0.4 for single exposure imaging at state-of-the-art 0.33 NA. Hence, flexible pupil shapes with small pupil fill ratio will be required to support these critical applications in high volume manufacturing.

Advances in illumination are aimed at generating arbitrary customized freeform pupil shapes, as well as regular dipoles or quadrupoles, with highest sigma and significantly reduced pupil fill ratio to support such low-k1 applications without light loss. Source mask optimization (SMO) can provide optimum pupil shapes leading to maximum process windows by compensating for imaging variations induced by rigorous mask effects, or to adjust the proximity behavior of the process.

Matching to currently used illuminators can be achieved with intelligent matching strategies.

For applications beyond the 5 nm node, the high NA anamorphic imaging and the associated flexible illuminator will enable even finer imaging resolution with single exposure EUV lithography. The use of anamorphic imaging has some interesting consequences on the definition and understanding of MEEF, which will be discussed as an outlook.

EUV Masks

Naoya Hayashi

DNP

Abstract not available at time of printing

Multi-Beam Mask Writer MBMW-101 for the 7 nm node, and beyond

Elmar Platzgummer

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The world's first high throughput multi-beam mask writer (MBMW) has been realized by upgrading the existing MBMW Alpha tool with a 10x faster data path. In this tool a multi-beam column provides 262k programmable beams; the current density is adjustable up to 1 A/cm², resulting in a total beam current of up to 1 µA. With the upgraded 120 Gbps data path a 7 nm node mask can be written in less than 10 hours.

The performance of the MBMW tool and its extendibility to future nodes will be discussed.

Stochastic and Non-Stochastic CD variations in Next Generation Lithography

Marie Krysak
Intel

Advancement of current patterning technologies is crucial as the semiconductor industry's demands for patterning smaller features at tighter pitches continue. Extreme Ultraviolet Lithography (EUVL) is expected to provide a substantial resolution gain over current 193nm processes. To simultaneously improve local CD variation, edge placement error and roughness, local resist variations must be considered. This talk discusses the fundamental resist performance limitations due to both photon and resist stochastics, and the state of current EUV materials in this context. In contrast, pattern roughness seen in directed self-assembly (DSA) processes is not driven by stochastics, but by inherent material characteristics. Challenges of introducing DSA to high volume manufacturing will be discussed.

Elements for EUV Electronic Resist Amplification

Deirdre Olynick,[1] Frank Ogletree,[1] Bo Xu,[2] Kristi Closser,[1] Oleg Kostko,[2] Musa Ahmed,[2] David Prendergast,[1] Daniel Slaughter,[2] Patrick Naulleau,[3] Paul Ashby,[1] Yi Liu,[1] William HInsberg,[4] Gregory Wallraff[5]

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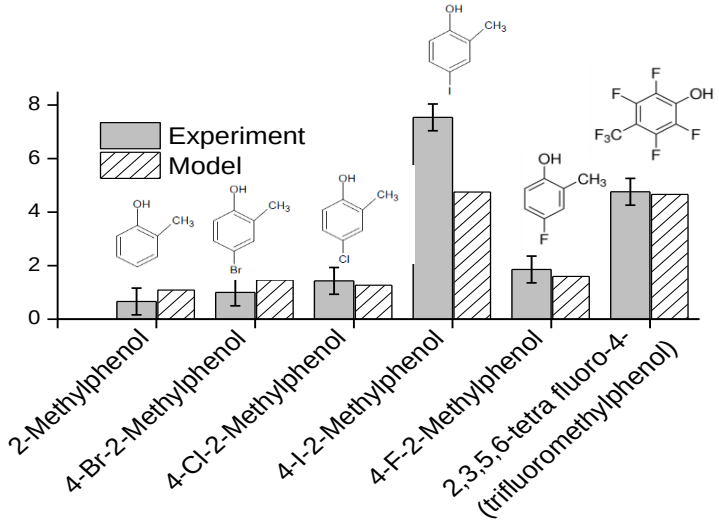
One of the biggest challenges of improving EUV resists is "seeing" the photon-induced reactions including the photo-induced electron cascade. The EUV cross-sections and binding energies for atoms are well known. This allows the prediction of photoemission cross-sections and photoemitted energies. However, this is only one important step in the process. Auger emission, molecular fragmentation patterns, and subsequent electron-resist interactions are also critical. These processes must be understood to control the material's EUV response and produce a high performance resist. We combine beam-line gas phase experiments of the EUV absorption with theoretical studies to gain fundamental understanding of the role of these processes in EUV radiation chemistry.

In this work, we present experimental and theoretical studies of resist analogs using tunable EUV radiation from the Advanced Light Source at Berkeley (ALS). Our equipment allows us to look at electron emission and photo induced fragmentation of resist components EUV irradiated in the gas phase. We study halogenated phenols with fluorine, chlorine, bromine, or iodine functionalization. We confirm that iodine is the highest cross-section absorption, but more importantly, we find that the photoemission is *amplified* beyond one electron. Results are summarized in Figure 1. With one iodine, the electron emission cross-section is increased relative to that calculated for photoemission alone (photoemission cross-section calculated using CXRO website[1]). This is due to Auger emission. Hence Iodine produces electrons beyond the primary photoemission for multiple electron emission per absorption event. . We will discuss these studies and accompanying theoretical work. In addition, we will describe our equipment capabilities which allow both EUV and electronic excitation of gas phase materials with detection of electron emission, low energy electron attachment, and molecular fragmentation. With this work, we can direct needed advancements in EUV resist design. This includes direction into which elements can "electronically" amplify the resist sensitivity.

Relative Electron Emission for a Series Halogenated Methyl Phenols



[1] http://henke.lbl.gov/optical_constants/

Session 6

Presentation Schedule for
Tuesday, November 8, 2016

Session Chairs
Geert Vandenberghe
Andres Torres

	Time	Presenter	Title
Session 6	7:00 – 7:25 PM	Yuri Granik (Mentor Graphics)	Gems and Jams of Inverse Lithography
	7:25 – 7:50 PM	F. Joseph Heremans (Univ. Chicago)	Localizing Point Defects in Wide Bandgap Semiconductors
	7:50 – 8:15 PM	René Klaver	Advantages of maglev stages for metrology and inspection applications
	8:15 – 8:40 PM	S.V. Sreenivasan (Univ. of Texas)	Emerging nanopatterning opportunities in electronics, displays, and healthcare
	8:40 – 9:05 PM	Martin Burkhardt (IBM)	Prospect of low-k1 Lithography in EUV
	9:05 – 9:30 PM	Robert R. McLeod (Univ. of Colorado Boulder)	Novel Multiple patterning lithography far beyond the diffraction limit
	9:30 PM	End Session	

Gems and Jams of Inverse Lithography

Yuri Granik, Mentor Graphics

One decade ago Inverse Lithography Technology (ILT) entered the roster of optical resolution enhancement techniques [1, 2]. Since then we accumulated, on one hand, numerous fascinating examples of ILT power and surprising ingenuity. On the other hand, certain shortcomings hinder wide acceptance of ILT in the production environment. Here we present assorted examples of the ILT "gems" - interesting and unintuitive solutions to lithographic problems, alongside with the "jams" - challenging unsolved problems and annoying glitches.

In mid-80th Prof. Saleh and his students (see [3] in particular) showed that under Nyquist frequency constraints a one-dimensional pattern can be printed exactly on target. We later proved that such a feasible pattern can be imaged by many different masks [4]. The real designs though consist of two-dimensional polygons; such non-smooth shapes with corners cannot be printed on target in principle. Multiplicity or absence of solutions means that the inverse lithographical problems are generally ill-posed, and require artificial regularization.

ILT packages are armed with distinct regularization techniques. For the user, this difference manifests itself in the different mask styles while imaging the same target shapes. We offer peculiar examples of mask styles for optimal corner printing.

In part, ILT research was commenced and sponsored by the manufacturing company [5] that ventured to introduce Chromeless Phase Lithography into metal layer production for 65 nm node. Pixel-based optimization produces unusual masks that look unrelated to the design but eventually do image the desired metal lines.

Complex Source-Mask Optimization illuminators tend to induce the waviness of printing contours along a weak dipole direction. While regular OPC could not suppress these oscillations, pxOPC (which is Mentor Graphics ILT product) automatically found an original solution.

In one of the next generation projects the Directed Self-Assembly guiding patterns are envisioned to be printed using 193 nm immersion machines. The specification for printing fidelity of guiding patterns is remarkably tight - about 1 nm - over a wide variety of densely and sparsely laid out double and single contacts. We demonstrate mask configurations and optical settings that achieved this goal.

In the advanced via and contact layers one of the main ILT challenges is to maintain compliance with mask-making rules. Obeying the minimum corner-to-corner constraint on staggered contacts often weakens printing fidelity and process variability band. We show examples where introduction of 45 degree edges helps to reconcile mask constraints and image quality.

If ILT is run full-chip, then the design cannot be processed in one piece, and has to be broken into the "chewable" chunks that are called tiles. In post-processing stage the tiles are stitched together; this may produce notches, jogs, and other undesirable artifacts. We discuss how this problem is being addressed.

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2. Y. Liu, et al., "Inverse lithography technology principles in practice…", SPIE BACUS, November 2005.
3. K. Nashold, B. Saleh, "Image construction through diffraction-limited high-contrast…", JOSA A, 1985.
4. Y. Granik, "On the uniqueness of optical images and solutions of inverse …", JM3, 2009.
5. V. Singh, et al., "Making a trillion pixels dance", SPIE Microlithography, 2008.

Localizing Point Defects in Wide Bandgap Semiconductors

F. Joseph Heremans[1,2], Paolo Andrich[2], Charles F. De Las Casas[2], David D. Awschalom[1,2]
1) Argonne National Lab, Materials Science Division, Lemont, IL 60439
2) Institute for Molecular Engineering, University of Chicago, Chicago, IL 60637

Point defects in wide bandgap semiconductors, such as the nitrogen-vacancy (NV) center in diamond, have shown excellent electronic spin properties which can persist up to room temperature. The spin associated with these defects can be manipulated and read out using a combination of microwave and laser radiation with techniques similar to those used in electron spin resonance (ESR). Researchers use these point defect spins as a test bed for quantum communication and quantum information processing schemes, as well as for atomic-scale electric, magnetic and thermal sensors. In the field of nanoscale metrology, the ability to localize these point defects is critical to achieve a sensor that is proximal to the surface of the crystal but still preserving long spin coherence and high sensitivity. A long spin coherence (T_2) is a figure of merit useful for quantum operations and quantum-assisted metrology.

Here we present lithographic and growth methods we utilize to precisely position single defect spins both in bulk material and in nanoparticles. These techniques range from top-down approach where we use ion implantation to force defects into the crystal, to a bottom-up approach where we grow the defects into the crystal itself.

In the case of creating NV centers via ion implantation, we implant nitrogen ions through apertures created with electron-beam lithography [1] to create small pockets of nitrogen-rich diamond along with a number of vacancies. We then anneal the crystal to diffuse the vacancies next to the implanted nitrogen atoms to form an NV center. The result is an array of NV centers (see figure on left) which have spin coherence times of $T_2 < 10$ µs and show an average of 1.4 NVs per aperture.

We have also developed a crystal growth technique that precisely controls the position of the NV center in both depth [2] and lateral directions [3]. These techniques separate nitrogen and vacancy formation by relying on the introduction of nitrogen source gas during the synthetic diamond growth to achieve a delta-doped layer of nitrogen rich diamond, with nanometer scale depth precision [2]. Subsequent electron irradiation create vacancies, and annealing techniques diffuse the vacancies to create NV centers within the delta-doped region of the diamond, at a specified depth. We observe that the depth of the NV center has a dramatic effect on the spin coherence time, with bulk-like $T_2 \sim 800$ µs occurring at depths > 50 nm.

We then achieve lateral localization in this scheme by replacing the electron irradiation with ion implantation of ^{12}C atoms through nanoscale apertures, to localize a cluster of vacancies. Through annealing, these vacancies diffuse to form individual NV centers within a volume of (~180 nm)^3 at a deterministic position. These shallow NV centers maintain long spin coherence times of $T_2 > 300$ µs [3].

For many sensing application, bulk diamonds are simply too large and diamond nanoparticles offer better spatial resolution and better proximal sensitivity. As such, we can extend these growth techniques to fabricate cylindrical diamond particles with finely-tuned and highly reproducible sizes (diameter = 100 to 700 nm). We demonstrate a DC magnetic field sensitivity of 9 µT/√Hz using these nanoparticles in a fluidic environment with a long-term optical trapping stability (>30 h) [4].

Furthermore, these techniques are not only limited to diamond. We have implemented these techniques with other point defects in wide bandgap semiconductors like the divacancy complexes in silicon carbide [5]. These lithography techniques enable us to locate point defects in wide bandgap materials both in bulk and nanostructures to realize scalable spin-sensing devices and coherent spin coupling mediated by photons and phonons.

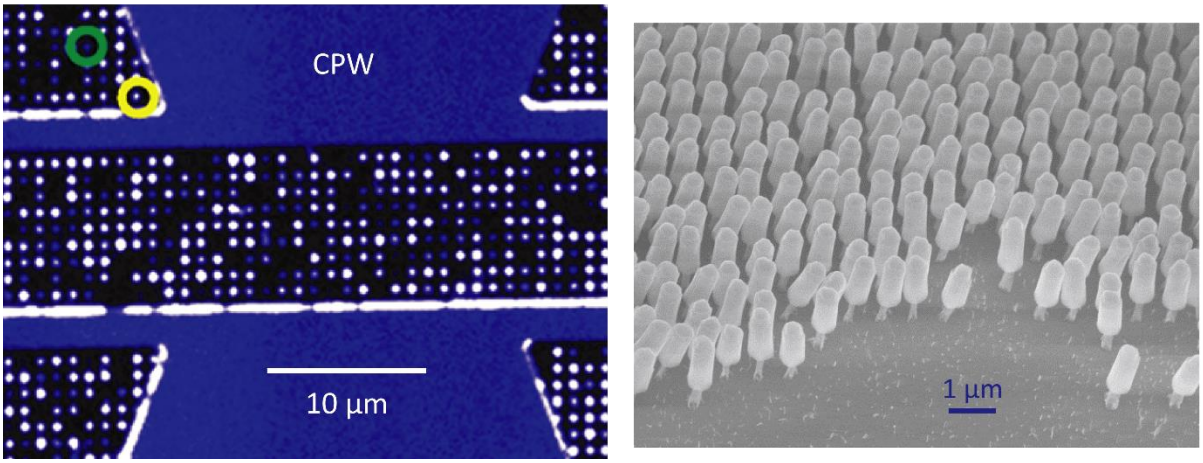

Figure: (left) A spatial photoluminescence scan of an array of implanted NV centers between a short-terminated coplanar waveguide (CPW) shown in blue, used to manipulate the spins of the NV centers. (right) Scanning electron microscope image of an array of 500 nm diameter diamond particles, with 700 nm pitch and ~1 µm height. The diamond particles are anchored to the underlying substrate with a pillar of photoresist.

We thank Kenichi Ohno and David M. Toyli for their initial experimental contributions.

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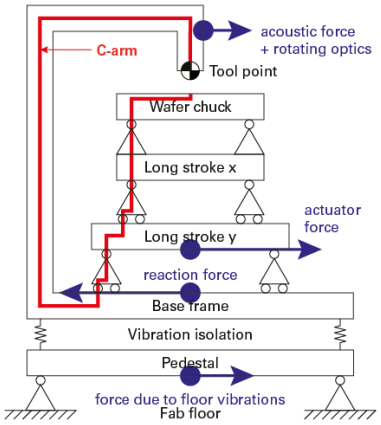
Advantages of maglev stages for metrology and inspection applications

René Klaver and Arjan Bakker
HEIDENHAIN NUMERIC B.V., Eindhoven, The Netherlands

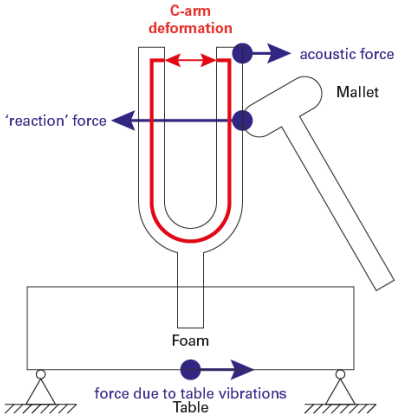
At HEIDENHAIN in The Netherlands, motion systems based on magnetic levitation (maglev) are developed, which target metrology and inspection applications. The reason for this development is that HEIDENHAIN sees many advantages of maglev wafer stages over conventional wafer stages. Maglev stages are characterized by their floating wafer chucks with zero-stiffness, conventional stages by their use of high-stiffness bearings, such as mechanical or air bearings. Some of the advantages of maglev stages over conventional stages are easy to explain: vacuum-compatibility and cleanliness (non-contact and therefore no particles). However, one of the more important advantages, the short settling time, is more difficult to explain. We will try to explain the short settling time in this presentation.

For that explanation, all tools which contain a wafer stage are modelled as tuning forks, as shown in the figures below. The reaction forces, caused by the acceleration or deceleration of the stages, are modelled as impulses with a mallet. With this model, the influence of stage accelerations on systems with conventional stages and maglev stages is determined: the tuning fork in the upper figure needs more time to settle compared to the tuning fork in the lower figure. In addition to quantitative results based on that model, we will present measurement results on the settling times of systems with our maglev stages and conventional stages.

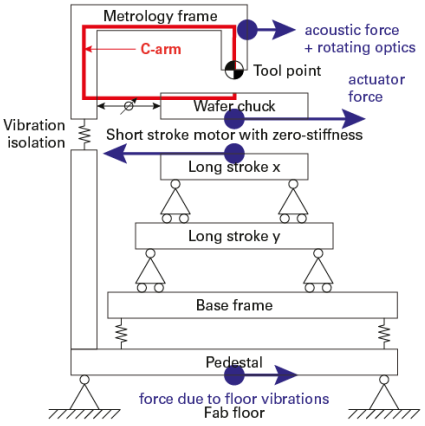
Tool with conventional wafer stage



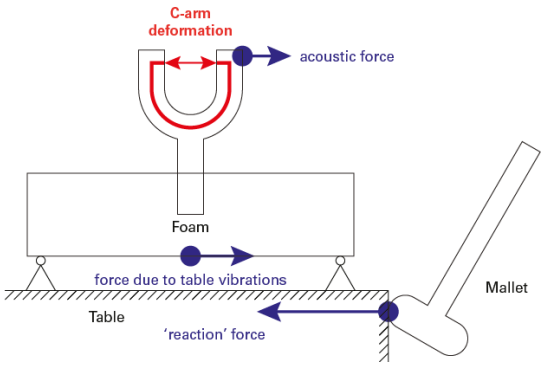
Equivalent with tuning fork and mallet



Tool with maglev wafer stage



Equivalent with tuning fork and mallet



Emerging nanopatterning opportunities in electronics, displays, and healthcare

S.V. Sreenivasan
(Univ. of Texas)

Abstract not available at time of printing

Prospect of low-k1 Lithography in EUV

Martin Burkhardt
IBM Research, Yorktown Heights, NY

The path of pre-EUV optical lithography has been stellar, culminating with routine printing of 80nm pitch patterns using ArF immersion scanners at 1.35 NA. This corresponds to a k_1 factor of 0.28, close to the theoretical limit. The imaging is so good, in fact, that it is possible to print at such high resolution even in two dimensions [1]. The first production-ready EUV scanners feature an NA of 0.33, and the pitch that can routinely be printed with large process windows is roughly 36 nm, corresponding to a k_1 of 0.44. While we have seen pitches smaller than 36 nm, we have not seen any claims of large process windows at 23nm pitch, which would be equivalent to what has been achieved with ArFi. And while it is certainly true that the materials teams have not had sufficient time yet to develop better materials for EUV, we also have to admit that the image that the scanner delivers is impacted by fundamental limitations due to the soft X-ray wavelength of the EUV systems.

The off-axis optical design around the reflective photo mask causes some of the problems associated with low-k_1 EUV lithography, such as horizontal-vertical bias, and telecentricity related issues caused by the angle-dependent mask reflectivity. Some of these problems can be solved by choice of mask multi layer stack, or mask absorber [2]. Another requirement for low-k_1 imaging is an intrinsic high contrast in 1d gratings. A high contrast and an associated image slope reduces line edge roughness and ultimately enables low-k_1 imaging for 2d features such as contact holes.

For low-k_1 lithography at EUV wavelength, the contrast is limited by the fact that each pole of a dipole illuminator produces shifted wafer images, the sum of which creates the final lower contrast image [3,4]. Each pole of the dipole delivers an image that is superior in contrast to that imaged by the combined dipole. This effect is due to the phase shift of light in proximity to the absorber, and therefore due to the dielectric constant of the absorber material. In fact, it is possible to remove this relative shift to a large extent by choosing an absorber with dielectric index closer to unity, such as aluminum. While this solves the problem of image separation of the individual poles, the choice of aluminum as absorber yields a degraded image for other reasons. One possible reason is the fact that since Al is nearly index-matched to vacuum, light incident at grazing incidence is not totally reflected in vacuum anymore, and instead enters the absorber, to be lost for imaging. To circumvent these limitations we are exploring the impact that the absorber diffractive index and thickness has on complex diffraction orders and image contrast. The various techniques for choosing an absorber stack will be highlighted in this presentation.

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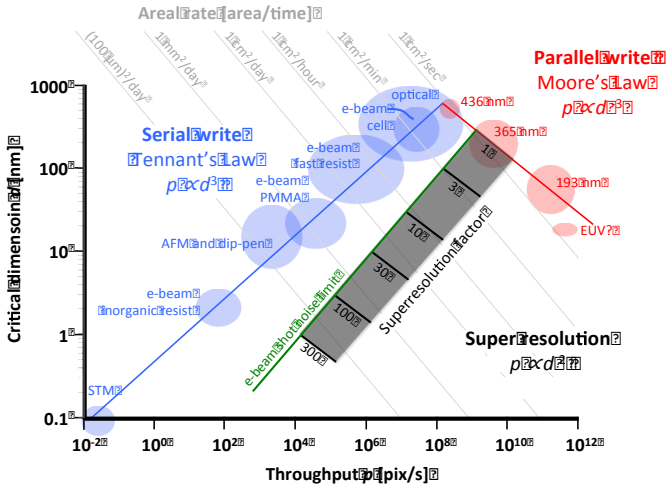
Novel Multiple patterning lithography far beyond the diffraction limit

Robert R. McLeod
Electrical, Computer and Energy Engineering Department, University of Colorado Boulder

Stimulated emission depletion (STED) microscopy, recognized by the 2014 Nobel in Chemistry, has demonstrated 5 nm localization with 775 nm illumination, a factor of 50 below the diffraction limit. [1] This narrowing of the fluorescent spot created by a focused laser is accomplished by a second laser in a donut mode that stimulates emission in the periphery of the excited spot, leaving only a small "donut hole" of fluorescence. This remarkable result inspired multiple groups [2] [3] [4] to publish various resist materials that mimicked STED via one chemically-initiating wavelength whose response could be confined below the diffraction limit by a second inhibitory wavelength with a bright periphery and dark center.

Despite this exciting promise, translation of these resist demonstrations into lithography practice has been challenging. Most lithography demonstrations have exhibited important but modest improvements in critical dimension, [5] potentially due to diffusional blurring of the polymerization crosslinking reaction that enforces a strong lower limit to the CD. [6] Second, the laser direct write architecture significantly limits lithographic throughput. A final challenge is that the resist in this approach is required to automatically regenerate to a pristine unexposed state between the many multiple patterning steps required to place multiple super-localized features within the addressable diffraction limit.

As an alternative approach to address these challenges, I will suggest the use of existing photo-resist materials refreshed by an external stimulus, essentially reducing the materials problem to the same requirement as traditional multiple patterning. I will then describe a new approach to mask design and fabrication capable of projecting deep sub-diffraction features to the far field that are arbitrary within the constraint that they must be resolved at the diffraction limit. Using the same super-localization enhancement method employed by STED microscopy, this method trades some of the large throughput of modern resists and projection lithography tools for feature size, as shown in the scaling for a 365 nm system, below. The potential system performance may be interesting for small batch, mask writing and research environments needing nm-scale lithography with modest throughput.



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Session 7

Presentation Schedule for
Wednesday, November 9, 2016

Session Chairs
Shalom Wind
Pat Martin

	Time	Presenter	Title
Session 7	8:00 – 8:25 AM	Nikolaj Gadegaard (Univ. Glasgow)	Cell and Tissue Engineering Based on Micro- and Nanolithography
	8:25 – 8:50 AM	Ricardo Ruiz (HGST, a Western Digital Brand)	Line Roughness in Block Copolymer Thin Films for Lithographic Applications
	8:50 – 9:15 AM	John Fourkas (Univ. of Maryland)	Progress Report on Photoresist Development for Multicolor Lithography
	9:15 – 9:40 AM	Nicole Lindermann (Nanoscribe GmbH)	3D Printing for Photonics Applications
	9:40 - 10:05 AM	Andres Torres (Mentor Graphics)	Reducing error placement sensitivity to guiding pattern distortions in cylinder forming DSA by optimizing grapho-epitaxy guiding templates.
	10:05 – 10:35 AM	BREAK	

Cell and Tissue Engineering Based on Micro- and Nanolithography

Nikolaj Gadegaard
Division of Biomedical Engineering, University of Glasgow, UK.

Background

The advances of semiconductor processing have fuelled the technical revolution of the 20th century, yet these advanced are increasingly seeing use outside the field of mainstream semiconductor fabrication. In this talk, I will present and discuss the developments, mainly in Glasgow, of how the use of semiconductor processing has impacted on research and applications in areas of biomedical research. The interplay between biological cells and manmade materials has intrigued researchers for nearly a century. However, it was not till the 1980's when semiconductor lithography made its introduction into the area of cell engineering. At that time it became possible to make artificial or engineered surfaces with dimensions comparable or smaller than cells and at the same time a high degree of lateral and vertical dimensions, through lithography and etching respectively.

Lithography

A great deal of interest has centred on length scales below 1 µm and with the requirement of customisable designs, electron beam lithography (EBL) is the main driver the majority of the research and through careful design and processing large areas (>10 cm^2) can readily be realised. A convenient lithography route for manufacturing features around 100 nm is the exposure of discrete dots placed in arrays. The conventional route is to have these dots placed in regular arrays but we have developed routines where the dots can be placed in highly specified geometries benefitting from the high placement accuracy available in EBL. Indeed we have demonstrated that by carefully controlling the placement geometry of the dots, the fate of adult stem cells can be controlled[1]. We have found that by introducing a small amount of random noise of the position of the dots (+/- 50 nm) the stem cells will differentiate into bone forming cells without any other stimulus than the surface topography, Figure 1.

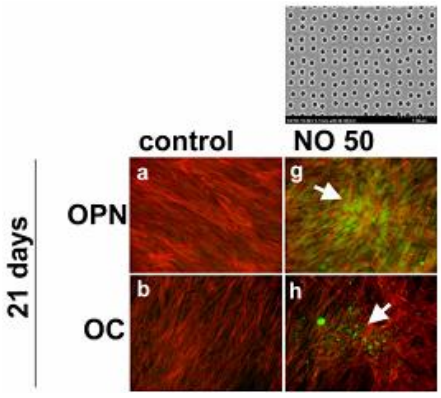

Figure 1. Introducing a small placement error induces

Gradient fabrication

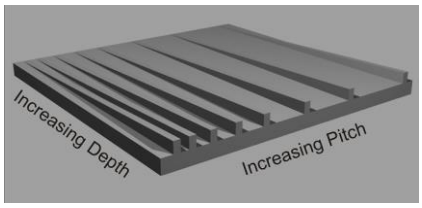

Figure 2. Gradient substrate with opposing

Not only are the lateral dimensions important in the guidance of the cells, but also the vertical dimensions. These are readily controlled by reactive ion etching, however, each iteration of the height requires both a lithographic and etch step making this approach slow. Thus we developed a process whereby a sacrificial polymer gradient was deposited across a predefined lithographic pattern which subsequently could be transferred to the substrate in a single etch step[2], Figure 2.

Polymer replication process

Although many of the processes widely used in semiconductor processing can be applied to biological applications, a number of new materials and processes have been developed to meet the requirements from life sciences. The materials may not be toxic, which excludes certain metals and semiconductors (e.g. III-V materials), they should ideally be transparent for optical microscopy to be carried out and if to be used in the body

have suitable mechanical properties – yet the materials must be compatible with clean room processes. A further demand from biological experiments is sample numbers, which calls for a reliable and fast replication process. We have specifically focused on polymer injection moulding where it is possible to produce 1-2000 samples in a lab scale environment. The whole process requires a master structure to be manufactured using EBL. From the master, a negative metallic replica is produced by electroplating which is fitted in the tool of the injection moulding machine. Polymer is then injected into the tool and a polymer replica is made against the electroplated insert, Figure 3. Polymers are ideal materials for biological used as they can be made transparent, have low cost and are non-toxic to the cells[3].

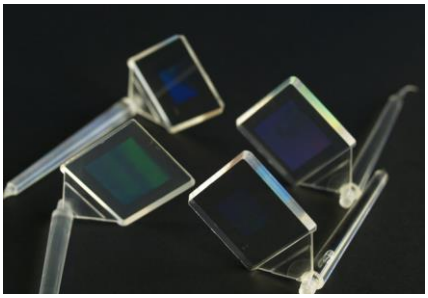

Figure 3. Injection

Biological examples

In the stem cell example above we found that the geometric layout of the nanodots played a critical role in the differentiation of the stem cells. An example for the use of gradient generated patterns is shown in Figure 4. Here we placed two different cell types, endothelial cells and fibroblasts, on a substrate with nanopillars of varying height[2]. From the experiment we could determine an optimal design for the separation of the cells. By extending our fabrication process, we have been able to manufacture nanopillars with an aspect ratio of 20:1 in polycarbonate using injection moulding. Such pillars (100 nm diameter) are flexible and can be distorted by the cells when moving across the surface, Figure 5. Such substrates have apparent lower mechanical properties and can be used to control the differentiation of cells too[4].

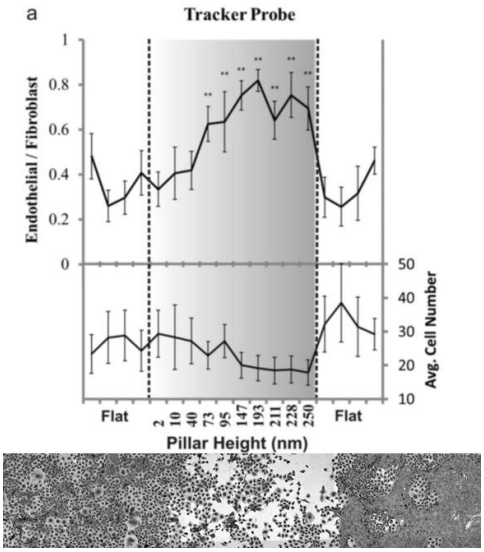

Figure 4. Separation of two

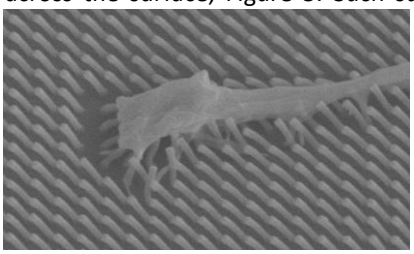

Figure 5. Cell extension bending the nanopillars as

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[1]Nature Materials 2007, Nature Materials 2011
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[3]Macromolecular Materials 2012, Journal of Micromechanics and Microengineering 2014
[4]Advanced Functional Materials 2016

Line Roughness in Block Copolymer Thin Films for Lithographic Applications

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In this talk, we review the work done at HGST over the years on line roughness in block copolymer films for lithographic applications. First, we look at thermal fluctuations as the source of roughness in un-directed, “fingerprint-like”, thin films. We propose a phenomenological model based on bilayer membrane formalism which includes adjacent layer correlations to explain the structure of the power spectral density. We study the characteristic correlations between line width and line placement roughness, which in turn determine the line edge roughness. Second, we study the observed line roughness in directed assembly when using chemical contrast guiding patterns. We look at the effect of the guiding patterns and the interplay with the “intrinsic” thermal fluctuations explained above. Third we look at the observed differences in perceived line roughness for various polymer pitch values and for various density multiplication values. Lastly, we evaluate the evolution in roughness during pattern transfer and discuss on the components of the power spectral density that remain from the original block copolymer film and what features are changed depending on the pattern transfer method. We hope these studies contribute towards establishing a comprehensive framework to understand the sources of line roughness in block copolymer lithography as well as understanding what properties can be engineered to achieve the tight specifications needed for semiconducting or magnetic device fabrication.

Progress Report on Photoresist Development for Multicolor Lithography

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John Petersen
Periodic Structures, Inc.

Multicolor lithography is a promising approach for the patterning of negative-tone photoresists with resolution in the tens of nm range using light in the visible or near ultraviolet.[1] This approach is progressing from its original, two-color schemes to more advanced 3-color schemes that offer substantially better resolution and a greater degree of flexibility in the patterning process.

The development of industrially relevant multicolor photoresists will require the development of versatile and highly controllable photochemical approaches. We have developed a new analytical method called the 2-beam initiation threshold (2-BIT) technique that is a powerful means of probing the linear and nonlinear chemical and optical dynamics of photoresists *in situ*.[2] 2-BIT is providing important new insights into the detailed photochemical processes occurring in existing multicolor photoresists, and is helping to drive our development of the next generation of multicolor photoresists with improved performance.

1. "2-Colour Photolithography," John T. Fourkas and John S. Petersen, *Phys. Chem. Chem. Phys.* **16,** 8731–8750 (2014); DOI: 10.1039/C3CP52957F
2. "In Situ Measurement of the Effective Nonlinear Absorption Order in Multiphoton Photoresists," Zuleykhan Tomova, Nikolaos Liaros, Sandra A. Gutierrez Razo, Steven M. Wolf and John T. Fourkas, *Laser Photon Rev.* (in press); DOI: 10.1002/lpor.201600079

3D Printing for Photonics Applications

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Photonics applications often require 3D freeform shapes for specific tasks like beam forming, focusing or light guiding. Additive manufacturing of photonic components is a rather new trend that showed its potential in recent breakthroughs. Macroscopic optics can meanwhile be fabricated by commercially available 3D printers form e.g. Luxexcel and Keyence. Two photon polymerization (TPP), however, is considered the most promising technology for 3D printed micro-photonics applications [1]. This talk will expand on TPP and it's applications in photonics, in particular we will discuss micro optics, 3D photonic crystals, as well as photonic wire bonds.

In the last decade, additive manufacturing based on two photon polymerization has set new standards for three-dimensional (3D) microfabrication. Due to its sub-micrometer spatial resolution, the technique provides the surface smoothness and shape accuracy required for high-quality optical elements. Almost arbitrary shapes with sub-micrometer feature size can be created direct from 3D digital models. Recent technological improvements have sped up TPP by more than a factor 100 while preserving its accuracy and resolution. High precision scan optics in combination with material research allow for ultrafast and precise solidification of the liquid resin and simultaneously secure mechanical stability, structural conformity and optically smooth surfaces (printer is commercial available [2]). Sophisticated embedded writing strategies additionally made the fabrication time drop to a fraction.

Due to this speed up, TPP fabrication of micro-photonic components with tailored shapes in millimeter to centimeter size arrays is now possible. Arrays with 100% filling factor, as well as hemispheres with vertical walls can be achieved. Micro-optics including lenses, cones, wedges and micro-pyramid arrays with less than 10 nm RMS roughness have been demonstrated. Those can be either used directly or as a master for molding and casting.

Taking advantage of the unparalleled 3D resolution and design freedom 3D photonic crystals [3] can be fabricated in TPP to investigate novel photonic phenomena. The technology allows for new photonic devices that tackle real world challenges. Cloaking of metallic contacts on light emitting diodes [4] or solar cells are examples of the systematic development of novel optical functionalities in transformation optics that can now be materialized.

Finally, TPP enables novel photonic interconnection approaches for photonic multi-chip systems. While on-chip light generation, modulation and detection can be performed on different integration platforms, powerful optical systems only live on functional interaction of all those components. Multichip assemblies from known-good devices are a possible path to create such systems in cases where monolithic integration is not possible or unwanted. Exploiting our TPP technique, photonic wire bonds [5]–[7] - miniaturized 3D interconnect waveguides - have been demonstrated to interconnect devices form different photonic integration platforms. Photonic wire bonds have the potential to reduce space, energy and cost of photonic multi-chip system assembly.

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[6] N. Lindenmann, S. Dottermusch, M. L. Goedecke, T. Hoose, M. R. Billah, T. P. Onanuga, A. Hofmann, W. Freude, and C. Koos, "Connecting silicon photonic circuits to multicore fibers by photonic wire bonding," *J. Light. Technol.*, vol. 33, no. 4, pp. 755–760, 2015.

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Reducing error placement sensitivity to guiding pattern distortions in cylinder forming DSA by optimizing grapho-epitaxy guiding templates.

J. Andres Torres, Joydeep Mitra, Polina Krasnova, Yuansheng Ma, Yuri Granik, Daman Khaira
Mentor Graphics Corporation

A key issue in enabling DSA as a mainstream patterning technique is the generation of grapho-epitaxy based guiding pattern (GP) shapes to assemble the contact patterns on target with high fidelity and resolution. Current GP generation is mostly empirical, and limited to a very small number of via configurations. Figure 1 shows results using a model-based GP synthesis algorithm and methodology for on-target and robust DSA. The final post-RET printed GPs derived from our original synthesized GPs are more resilient to process variations while conserving fidelity in terms of placement error and target shape.

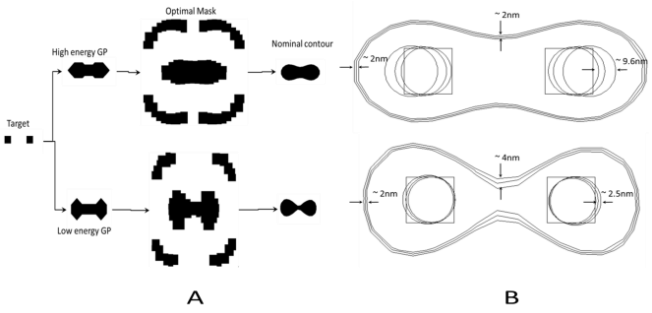

Figure 1. Suboptimal and Optimal guiding pattern synthesis. (Top) Shows the guiding pattern target generated by traditional means, the OPC and the resulting assembly under process variations. (Bottom) Shows the guiding pattern generated using an additional low-energy constraint and showing a more robust assembly behavior even under larger guiding pattern distortions.

In order for the model to produce more resilient guiding patterns, the model must provide a metric that permits to measure how far the assembly process is from the phase transition of the BCP under different confinement configurations. Figure 2 shows with the different data points the probability of failure of a given guiding pattern shape. The data is sorted in the x-axis from the lowest template internal energy (those deemed to be more robust) to the highest template internal energy (those which are undergoing phase transition).

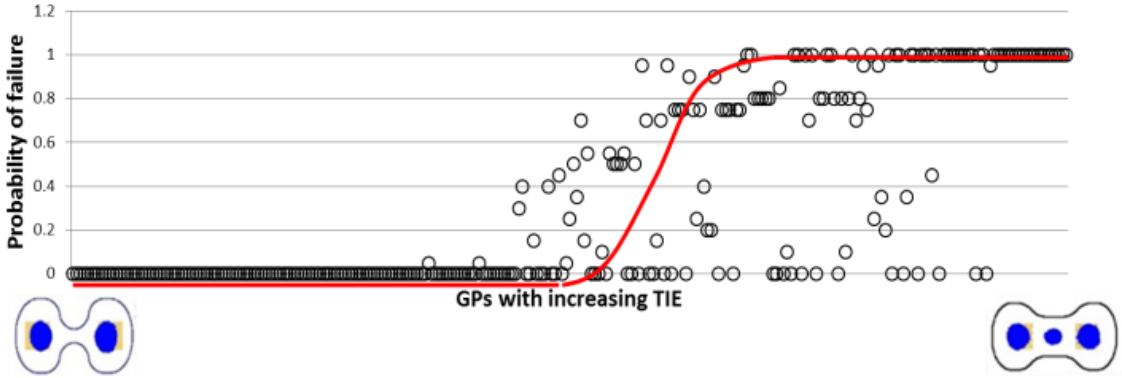

Figure 2. Probability of failure for different guiding pattern shapes. The shapes are organized from lowest Template Internal Energy (TIE) to highest TIE in the x-axis. The y-axis corresponds to the probability of failure, normalized to the total of number of performed simulations (in this case 100 per guiding pattern).

Full physics models cannot use the internal energy of the system as the total energy of the system will remain fairly constant by finding the minimum energy configuration. In other words, the total energy of the system depicted at the left and at guiding pattern depicted at the right of Figure 2, have similar total energy values, since their configurations have changed. In contrast, a compact model is designed to compute the energy assuming a fixed, desirable configuration, thus permitting finding higher than usual total energies, as the model itself prevents the system to adopt a different -more energy efficient- configuration.

However, the model and correction itself is not sufficient to find optimal guiding patterns for every target and BCP formulation combination. The desired pitch must be commensurable to the natural period of the material as Figure 3 suggests.

Figure 3A shows how the error placement under lithographic process variations using a 193i system has a maximum range of 2.4nm when using an optimal guiding pattern generation method. In contrast, if a sub-optimal solution is used the error placement can be in excess of 6nm.

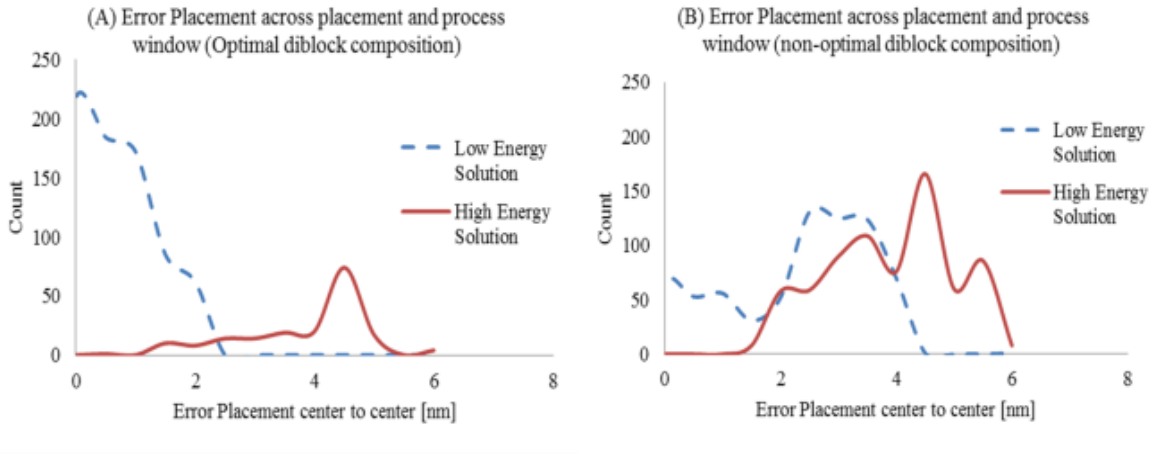

Figure 3. (A) Shows optimal BCP formulation for optimal guiding pattern (low energy solution), and sub optimal guiding pattern (high energy solution). (B) The BCP natural period had a mismatch between with respect to the intended target.

Figure 3B shows how even if the optimal methodology is used, if the natural period of the material is not commensurable to the desired pitch, the error placement is significantly higher when compared to the solution when both guiding pattern and BCP composition are optimized to find the more robust guiding pattern shape.

Session 8

Presentation Schedule for
Wednesday, November 9, 2016

Session Chairs
John Petersen
Doug Resnick

	Time	Presenter	Title
Session 8	10:35 – 11:00 AM	Uwe D. Zeitner (Fraunhofer-Institut für Angewandte Optik und Feinmechanik)	Alternative lithographic technologies for micro- and nano-optical applications
	11:00 – 11:25 AM	Britt Turkot (Intel)	
	11:25 – 11:50 AM	Dan Meisburger (Tec-Start Consulting)	The Maskless Lithography Revolution in PCB Production
	11:50 – 12:15 PM	Vassilios Constantoudis (NCSR Demokritos)	Line Edge Roughness is more than just roughness: Recent challenges in LER metrology
	12:15 – 12:40 PM	Hiroki Nakagawa (JSR)	Novel Spin-on Hard Masks Materials for 5nm Node and Beyond
	12:40 – 1:10 PM	Peng Liu (ASML Brion)	Modeling Challenges in Negative Tone Lithography
	1:10 PM	End Session	

Alternative lithographic technologies for micro- and nano-optical applications

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Compared to the lithographic realization of nano-structures for micro-electronics the demands of today's optical applications on the lithographic fabrication technologies are different. This relates to the lateral shape of the structures as well as to their three dimensional surface profile. On the other hand, optical nano-structures are often periodic which allows for the use of dedicated lithographic exposure principles not always applicable for the structuring of IC pattern.
In the presentation an overview of some actual lithographic technologies will be given specially developed for the realization of high resolution optical nano-structures. This includes a special electron-beam lithographic exposure technique for high-quality and high resolution sub-wavelength pattern generation, the diffractive mask aligner lithography for cost-effective fabrication of large area 3-dimensional optical nano-structures, and a flexible direct-write LED-Stepper 3D micro-optical surface profile realization.
Electron-beam lithography using the Variable Shaped Beam (VSB) writing principle is a suitable and very flexible fabrication technique to address the needs of optical applications. It is based on an exposure with extended geometrical primitives like rectangles or triangles of flexible size. In case of periodic pattern as they are found in optical elements like photonic crystals or meta-materials, the VSB writing principle can be further extended by a so called character projection where complex exposure pattern are coded in a stencil mask and exposed with a single shot. Resulting shot-count and thus writing time reductions can be in the order of about 100...10000. The realization of numerous kinds of elements on larger areas becomes possible only with such a highly parallel writing strategy. The flexibility for generating arbitrary pattern is maintained by a specially developed diaphragm stage offering to combine more than 500 different exposure characters in a single layout (see e.g. Fig. 1a).
The second technique to be discussed in more detail is the mask aligner lithography utilizing diffractive photo masks. It has opened a way towards a cost-effective fabrication of high resolution nano-structures with feature sizes well below 200nm. This approach thus overcomes the typical limitations of conventional shadow printing mask-aligner exposures and moves its resolution limit by at least one order of magnitude. In the last few years we have demonstrated the huge application potential of diffractive mask-aligner lithography by the realization of different micro- and nano-structures with demanding quality criterions such as highly efficient pulse compression gratings, wire-grid polarizers for wavelengths down to 400nm (see Fig. 1b), plasmonic absorbers, or non-periodic pattern with micrometer resolution.
In the contribution it will also be shown what could be the necessary next development steps for further improving the diffractive mask-aligner technology, especially towards the realization of three-dimensional surface profiles. For this purpose, we have implemented some additional changes in the mask-aligner. First, the conventional Mercury arc-lamp has been replaced by a specially designed laser illumination. It includes dedicated means for an effective speckle reduction and homogenization as well as a computer controlled scanning system. The second extension is a piezo-controlled lateral alignment between mask and substrate which allows performing multiple exposures with lateral shifting the mask by a given distance in between the single exposures. In combination with the pattern transfer by diffraction effects both modifications can be used generate locally varying exposure intensities and thus a three-dimensional surface profile after the resist development process.
It will be discussed that the key for addressing current and future demands of flexible high-resolution patterning – at least for optical applications – lies in the combination of different lithographic approaches. This could be e.g. a combination of e-beam lithography for diffractive photo-mask-fabrication, their use in advanced mask-aligner lithography, the combination with scanning beam principles for generating large area pattern without stitching artifacts, as well as the utilization of Atomic-layer deposition or self-aligned double patterning for fine-tuning of functional parameters.

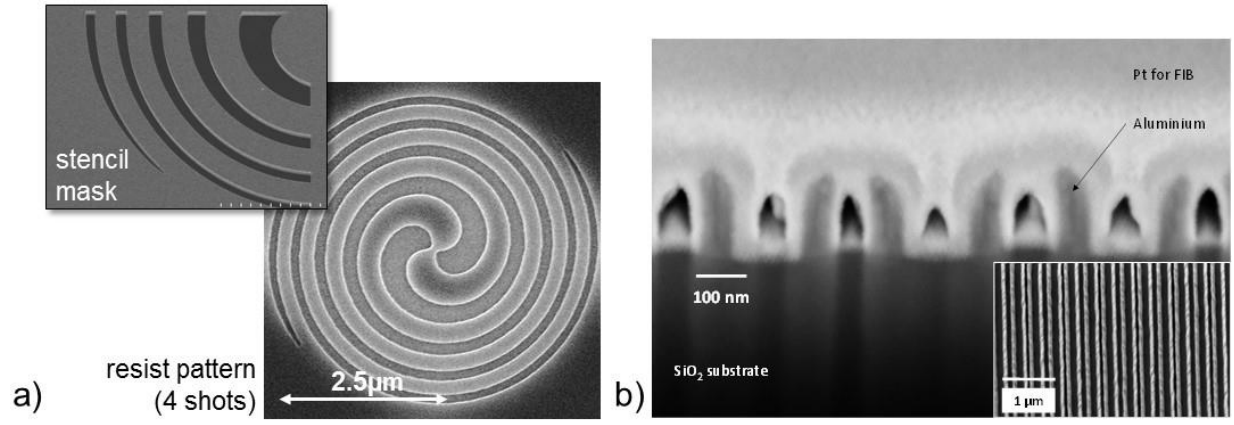

Fig. 1: a) Electron-beam lithography based on flexible character projection for high-throughput fabrication of repetitive nano-optical structures (here a microscopic vortex-lens). b) Wire-grid polarizer with sub-100nm feature size (175nm period) realized by Diffractive Mask-Aligner Lithography and self-aligned double patterning (SADP).

Title to be announced

Britt Turcot

Intel

Abstract not available at time of printing

The Maskless Lithography Revolution in PCB Production

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The printed circuit board manufacturing industry is in the early stage of a major lithographic transition from contact printers to direct-write (maskless) optical imaging systems with over 1,000 of these units shipped to date. The smart phone in your pocket, complex wireless and internet network boards, and many others, all depend on the special capabilities and advantages of maskless lithography. Because the PCB is sometimes considered to be "low tech", this ongoing revolution may have been overlooked by many in the semiconductor industry. While the line widths are large, the maskless systems are complex and in many ways more sophisticated than systems proposed for writing silicon.[1]

Unlike the historical progression of semiconductor lithography from contact printing to optical mask projection and then, maybe, to maskless lithography, the PCB industry has skipped mask projection except for interposers. The reasoning behind this difference, the special requirements of PCB lithography, and the performance of commercial maskless systems will all be discussed.

[1]Eric J. Hansotte, Edward C. Carignan, W. Dan Meisburger, Proc. SPIE **7932**, (2011)

Line Edge Roughness is more than just roughness: Recent challenges in LER metrology

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Institute of Nanoscience and Nanotechnology, NCSR Demokritos, Aghia Paraskevi, Greece &
Nanometrisis P.C., Aghia Paraskevi,

During the last decade, Line Edge Roughness (LER) attracted a lot of interest in semiconductor research and industry due to its critical role in the quality of printed lines and the yield of fabricated devices. Besides the research for the identification of its origins and the methods proposed for mitigation, several works contributed to LER measurement and characterization given the importance it has in achieving the ultimate aim of its control and reduction.

Being an aspect of roughness, LER metrology possesses all the complexities and ambiguities of roughness characterization. This was realized quite early in litho-metrology community and advanced characterization tools besides rms value, such as Power Spectral Density and correlation function and length, proposed and elaborated. In parallel, it was taken into account that the sidewalls come in couples defining the width of lines. Consequently, the random edge fluctuations cause variations of line width along lines and lead to the so called Line Width Roughness (LWR). One step further, the low-frequency part of contributes to CD variability while the high-frequency content of LWR can cause leakage and timing issues in circuit performance. The above description summarizes the conventional background to LER metrology and justifies the importance of advanced metrics (PSD, correlation functions and length).

Despite the early definition of c-factor between edges to quantify their possible correlations, the so far assumption in photolithography patterns has been that no correlations exist between edges and lines across line direction. However, modern lithographies (Directed Self-Assembly and Multiple Patterning) challenge both assumptions. The Line/Space (L/S) patterns they create are characterized by strong edge correlations (wiggling lines) and cross-line correlations whose characterization demands updated LER metrology to quantify these and control the placement errors they cause in IC manufacturing.

The aim of this talk is to outline an updated metrological scheme for LER endowed with concepts and metrics to capture the new features of lithographic patterns. Furthermore, we generalize an algorithm for the generation of synthesized SEM images with L/S patterns to include edge and cross-line correlations and aid the justification and exploration of novel metrics. First we define the notion of Line Center Roughness (LCR) whose low-frequency part is related to the local placement errors and show the distinct contributions of LWR and edge correlations to it (see Fig.1). Furthermore we adapt the three-parameter model of LER to LCR and show its relation to pitch variability. Then, we introduce the c-factor correlation function which quantifies the strength of the correlations between lines versus their horizontal distance in pitches. The meaning of v-factor function is illustrated and explained in synthesized SEM images with full control of their dimensional and roughness parameters (see Fig.2) and then applied to the analysis of experimental DSA and MP line/space patterns. Finally, we use the synthesized SEM images to investigate the effects of measurement and image noise on the new metrics and propose methods to mitigate these.

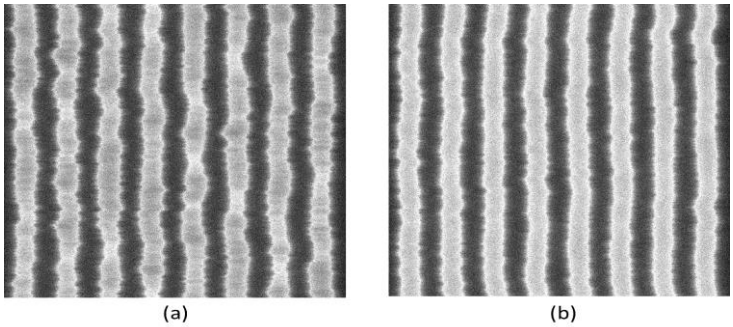

Figure 1. Synthesized SEM images shown line/space patterns with pitch=120nm and CD =50nm. Both patterns have exactly the same LCR (Rms_{LCR}=4nm) but differ in the main contribution to LCR. In (a) LCR is due to high LWR (Rms_{LWR}=7.7nm) since the edge correlations are reduced (c=0.04) whereas in (b) LCR comes from the strong edge correlations (c=0.83) since LWR is quite low (Rms_{LWR}=2.53nm).

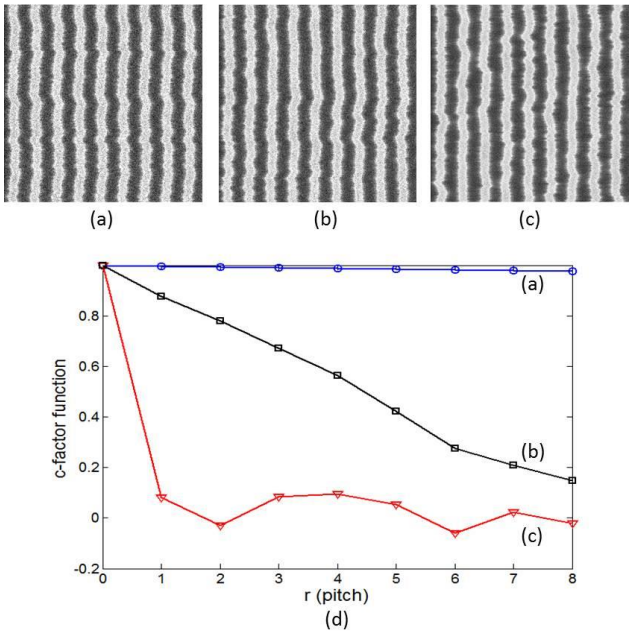

Figure 2. (a-c) Three synthesized top-down SEM images displaying patterns with reduced cross-line correlations from fully correlated in (a) to uncorrelated in (c); (d) the cff(r) of the images shown in (a-c) demonstrating the capability of cff to capture and quantify the amount and extent of cross-line correlations

Novel Spin-on Hard Masks Materials for 5nm Node and Beyond

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Spin-on hard masks are expected to play a crucial role in various lithography processes as well as in future semiconductor manufacturing integration schemes. The ArFi multi-patterning lithography process uses spin-on hard mask materials in underlayer processes to provide wide process windows by suppressing substrate reflectivity as well as etch-transfer of fine patterns to substrates by enhancement of etch selectivity. Recently spin-on hard mask materials were investigated as an alternative to CVD hard masks for several integrated processes since spin-on processing shows significant advantages for gap-filling and planarization performance to substrate topography. In this presentation, various JSR novel spin-on hard mask materials are introduced. Recent process made in wet strippable silicon hard mask for post etch processing, several metal hard masks with unique etch selectivity, and high thermal resistance organic hard masks will be discussed.

Modeling Challenges in Negative Tone Lithography

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Semiconductor manufacturers are increasingly adopting the negative tone lithography (NTL) in their leading-edge applications due to its superior imaging quality compared to the conventional positive tone lithography (PTL), particularly for small resist trench and contact/via patterns. While this adoption is critically needed in order to achieve the required process window for the ever-shrinking device feature sizes, it also brings new challenges to the computational lithography in terms of model accuracy, especially in full-chip applications such as optical proximity correction (OPC) and verification where the compact resist models are generally employed.

In order to print the same wafer target as PTL, NTL uses a negative tone imaging (NTI) process and a negative tone development (NTD) process as opposed to the positive tone imaging (PTI) process and the positive tone development (PTD) process used in PTL. The new modeling challenges arise from NTD not NTI. Note that NTI uses a mask of reversed tone of PTI (i.e., dark field is changed to bright field or vice versa), which introduces no new optical effects. Therefore, the mask and optical models that work well with PTI will work equally well with NTI. However, the situation is quite different between NTD and PTD. The engineers often find the resist model forms that have been working very well with the PTD process suddenly perform very poorly on the NTD process, because the resist behaves quite differently in NTD, much more than just the reverse tone in the resist dissolution rate. While the final resist profile in a PTD process is generally dominated by optical effects, it is not true anymore in a NTD process.

One of the very distinctive effects observed in NTD is the resist shrinkage induced by the de-protection reaction during the post-exposure bake (PEB). This effect is small in PTD because the resist volume having a high level of de-protection (and therefore high shrinkage) is removed by the developer and therefore may be ignored in PTD resist simulations. But this high-shrinkage volume is what remains in NTD. Therefore, a resist shrinkage model is required in NTD resist simulations.

Compared to PTD, the current NTD process has also shown quite different resist dissolution characteristics, such as a lower dissolution contrast with a smaller max dissolution rate and a larger min dissolution rate, as well as a stronger dependency of dissolution rate on pattern density (a.k.a. loading effect). Currently the Mack development model (or its inverse version) is the de facto industry standard used in PTD (or NTD) physical resist development simulations. Although this model is capable of taking into account the low contrast property, it inherently lacks the mechanism for the strong loading effect observed in NTD. A more rigorous physical resist development model is required to capture this effect.

In this work we discuss the first-principle approach to address these modeling challenges. For a given process, we first make educated assumptions about the fundamental physical/chemical mechanisms or laws that govern its behaviors. Then we derive the mathematical representations of these mechanisms, often in the form of, although not limited to, partial differential equations. These mechanisms and their mathematical representations are collectively referred to as the model for the given process. It can be applied to specific use cases to predict their behaviors. Specifically, we assume that the resist shrinkage process is governed by the mechanisms as illustrated in Fig.1 and the resist development process is governed by the mechanisms as described in Fig.2. We will present the development of the models for these processes and their simulation results.

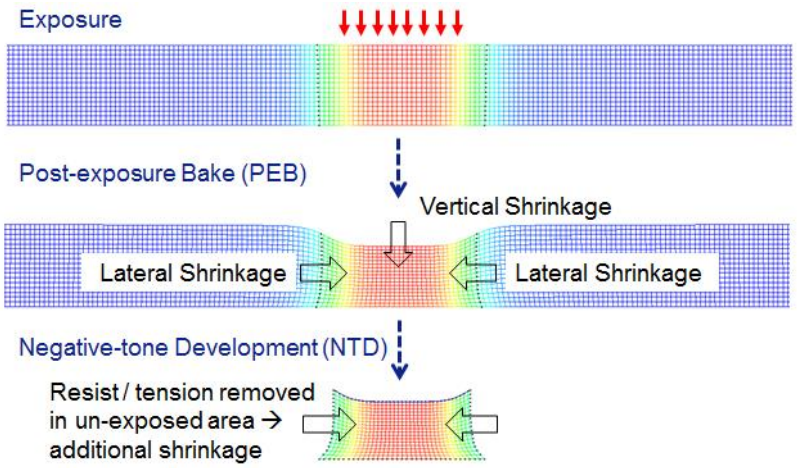

Fig.1 Resist shrinkage process & mechanisms: Acid is produced in resist exposure. It catalyzes the de-protection reaction in PEB. The volatile by-products evaporate, causing initial strain/stress in resist. The resist deforms to relax the stress, which eventually brings the system to the equilibrium state as determined by the theory of elasticity.

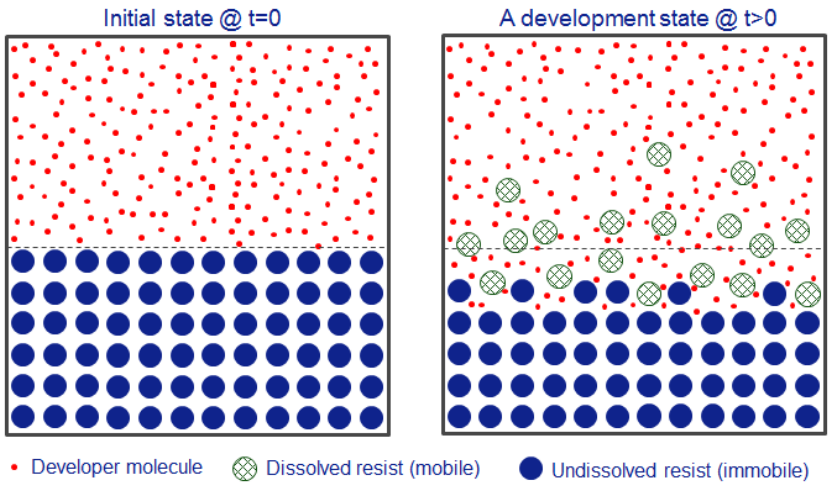

Fig.2 Resist development process and mechanisms: The developer diffuses into and reacts with the resist. It turns the undissolved resist into dissolved resist, which then diffuses away. It is also assumed that the dissolution reaction depletes the developer and slows down the dissolution rate. The developer has to be replenished via diffusion and this diffusion process can be affected by the interaction with the dissolved resist.

Session 8B

Presentation Schedule for
Wednesday, November 9, 2016

Session Chairs
Luigi Capodieci
Kevin Lucas

	Time	Presenter	Title
Session 8b	2:30 -2:55 PM	Andrew Khang (UC San Diego)	Measuring the Design ROI of Patterning Technology Options
	2:55 – 3:25 PM	Christopher Ober (Cornell Univ. / JSR)	EUV metal oxide photoresists: Finding common features between systems
	3:25 – 3:50 PM	Eric Hendrickx (imec)	Accurate modeling of EUV mask 3D effects and possible mitigations
	3:50 – 4:15 PM	Ryan Wicker (Univ. of Texas El Paso)	Printing Multi-Functionality using Additive Manufacturing
	4:15 – 4:40 PM	Soichi Owa (Nikon)	Optical lithography potential innovations with near-term feasibility

Measuring the Design ROI of Patterning Technology Options

Andrew B. Kahng

UC San Diego CSE and ECE Departments
Website: http://vlsicad.ucsd.edu/~abk/
Email: abk@ucsd.edu

At the N7 foundry node and beyond, the many available options for patterning technology and IC layout design styles together make design-technology co-optimization for "ultimate PPAC" extremely challenging. How many BEOL layers should be at 1X, 2X etc. pitch (and what about unidirectionality vs. bidirectionality)? How does the PPAC envelope change between 6T and 7.5T library enablements? How can circuit and layout design extract the maximum possible benefit from airgap enablement? (And so on.) The economic well-being of the industry requires that these and similar questions be answerable early in technology planning, in a design-agnostic and EDA flow-agnostic manner. This talk will point out some recent work toward this end: (i) a "PROBE" framework for rank-ordering of BEOL stack and design enablement options, (ii) studies of cell architecture and airgap options, (iii) studies of cut mask and block mask tradeoffs, and (iv) "optimal" placement, routing and other solvers as a foundation for such studies.

Speaker Bio: Andrew B. Kahng is Professor of CSE and ECE at UC San Diego, where he holds the endowed chair in High-Performance Computing. He has served as visiting scientist at Cadence (1995-1997) and as founder/CTO at Blaze DFM (2004-2006). He is the coauthor of 3 books and over 400 journal and conference papers, holds 33 issued U.S. patents, and is a fellow of ACM and IEEE. He has served as general chair of DAC, ISQED, ISPD and other conferences. His research interests include IC physical design and performance analysis, the IC design-manufacturing interface, combinatorial algorithms and optimization, and the roadmapping of systems and technology.

EUV metal oxide photoresists: Finding common features between systems

Christopher K. Ober [1)], Kazuki Kasahara [2)], Hong Xu [1)],
Vasiliki Kosma[1)], Jeremy Odent [1)], Emmanuel P. Giannelis[1)]

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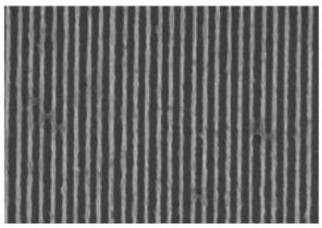
[2)] JSR Corporation, Semiconductor Materials Laboratory, Fine Electronic Research Laboratories, 100 Kawajiri-cho, Yokkaichi, Mie, 510-8552, Japan

EUV lithography remains one of the most promising candidates for next generation lithography with its potential high resolution. The main challenge for EUV resist design is to satisfy the aggressive resolution, line-width roughness (LWR) and sensitivity targets outlined in the ITRS roadmap. Limited light sources and unusual absorbance characteristics make the creation of EUV resists a complex challenge. The performance targets require development of entirely new resist platforms and several research groups in academia and industry have begun to explore metal organic photoresist materials.

Metals offer the possibility of a larger photoabsorption cross-section at EUV wavelength in a metal resist than conventional organic photoresist materials. There is some evidence that metal and metal oxide systems harvest the high-energy radiation and transfer it to other components in a photoresist to ultimately make the solubility change. Overall the metal and metal oxide systems follow the same LWR trade-offs seen in organic chemically amplified resists, that is, when exhibiting high sensitivity, they have lower resolution and vice versa.

Cornell University has studied metal oxide nanoparticle photoresists for EUV patterning. A range of hafnium and zirconium oxide nanoparticles with PAG exhibit sub 30nm line negative tone patterns at an EUV dose below 5 mJ/cm2, showing one of the best EUV sensitivity results ever reported. In this paper, recent progress in nanoparticle photoresists will be described. Discussion regarding new metal core applications and mechanism studies will be included in the context of known, published metal and metal oxide systems.

Regarding metal core studies, new metal elements have been applied to nanoparticle resist systems in terms of high EUV absorbance for better lithography performance. In particular, new zinc oxide nanoparticles have shown better resolution than zirconium oxide nanoparticles. E-beam and EUV exposure results of these new photoresists will be described. In study of the patterning mechanism, (1) ligand exchange, (2) ligand dissociation and (3) condensation reactions are all considered to occur in parallel. However, these plausible mechanisms were investigated in experiments using DUV exposure. Improved mechanistic understanding derived from e-beam and EUV exposures will be discussed.



CD=26nmL, 4.2 mJ/cm^2

Figure 1. Extremely High EUV sensitivity using Cornell University's nanoparticle photoresist

Accurate modeling of EUV mask 3D effects and possible mitigations

Vicky Philipsen[a], Iacopo Mochi[a], Emily Gallagher[a], Eric Hendrickx[a] ,
Kateryna Lyakhova[b], Friso Wittebrood[b], Guido Schiffelers[b], Timon Fliervoet[b]
[a] imec [b] ASML

In EUV lithography, the interaction between light of 13.5nm wavelength and mask features generates strong mask 3D effects. On wafer, the mask 3D effects manifest themselves as pitch-dependent best focus positions, pattern asymmetries and image contrast loss. To understand, and where possible, mitigate the mask 3D effects, rigorous and accurate modeling of the mask 3D effects is needed.

Using experimental techniques, such as X-section of the EUV mask films, EUV reflectometry and mask 3D AFM, accurate models have been built for standard EUV masks. These models have been validated using experimental results for standard mask technology, which uses a Ta-based absorber. For example, the models accurately match the experimentally observed best-focus shifts for line-space patterns at different pitches, or the experimental CD asymmetry in two-bar patterns.

To minimize the mask 3D effects, we discuss two possible techniques. For masks having a standard Ta absorber stack, we explore the use of assist features with different sizes and locations. The assist features are placed next to isolated features and two-bar structures, consistent with N7 node designs for 0.33NA and different off-axis illumination settings. For these generic N7 structures, wafer imaging will be compared to simulation results and an assessment of optimal assist feature configuration will be made.

As a second technique to mitigate M3D effects, we discuss a more complex change to mask technology; replacing the Ta absorber of the current EUV mask with a metal of higher absorptivity or refractive index closer to 1. Thin metal films deposited on wafer have been characterized for their composition and optical properties. The reduction to the mask 3D effects associated with the absorber modifications can be predicted using the calibrated models and the collected film properties. The relative need for, and impact of, these two mask 3D mitigation methods is compared.

Printing Multi-Functionality using Additive Manufacturing

Ryan Wicker, Ph.D., P.E.
Mr. and Mrs. MacIntosh Murchison Professor and Director
W.M. Keck Center for 3D Innovation

University of Texas at El Paso
El Paso, Texas 79968

Since the commercial introduction of Additive Manufacturing (AM) technologies nearly three decades ago, considerable advancements in processing speed, accuracy, resolution and capacity have been achieved and the available AM materials have expanded considerably, enabling customized end-use products to be directly manufactured for a wide range of applications. Many AM technologies have been released that use different processes for fabricating the individual layers from a variety of liquid, solid, and powder-based materials including polymers, metals, ceramics, composites, and more. In 2000, the University of Texas at El Paso identified AM as an emerging technology and invested strategically in establishing the W.M. Keck Center for 3D Innovation (Keck Center). The Keck Center has grown to occupy over 13,000 sq. feet with more than 50 commercial and custom AM machines. One particular focus of Keck Center research is on developing the methods and systems required to have automated control over material placement and structure creation to fabricate, for example, complex 3D devices that integrate electronics within mechanical structures. There are myriad issues associated with combining multiple materials to create functional products – from the deposition and processing of different materials to the combined performance of the materials in the resulting product. Despite these issues, the opportunities for AM in aerospace, defense, biomedical, energy and enumerable other applications continue to expand as the achievable length scales in AM decrease, the number of materials available for use in AM increases, the performance of these materials are characterized and controlled in the final product, and new strategies for integrating AM with other manufacturing technologies are successfully demonstrated.

Optical lithography potential innovations with near-term feasibility

Soichi Owa
Nikon Corporation

Historically, next generation lithography (NGL) has been explored seeking for finer resolution scaling, by changing wavelength or by changing basic mechanism. EUVL, EBDW, NIL and DSA are typical technology options discussed to date. Scaling is expected to increase the value of IC chip, at the same time, reducing production cost, resulting in the improvement of value productivity.

There exist, however, other potential innovation ideas to improve the value productivity, which are within the category of optical lithography, keeping basic resolution performance. Since they are close to existing technology, near-term feasibility is expected. In this paper, two options of such ideas are discussed.

One is 450 mm wafer scanner, which improves the productivity of wafer processes. I will show the latest performance data of NSR-650D, the first operating 450 mm scanner, such as mix and match overlay accuracy.

The other idea is optical maskless, which improves the cost of mask making. This technology, if successful, will be an example of general trend of digital imaging; such as, digital camera, PC projector, and so on. Feasibility study teaches us that currently available throughput of optical maskless is lower than that of conventional mask scanners, so that the initial use will be limited to IC device prototyping or other special purpose manufacturing. I will discuss key points of this technology.

Session 9

Presentation Schedule for
Thursday, November 10, 2016

Session Chairs
Deidre Olynick
Ralph Dammel

	Time	Presenter	Title
Session 9	8:00 – 8:50 AM	Richard Schenker (Intel) ***Keynote Speaker***	Foundations for 3nm half-pitch patterning
	8:50 – 9:15 AM	Patrick Shiavone (Aselta)	Why we should escape 1D-centric e-beam lithography flow
	9:15 – 9:40 AM	Leo Pang	GPU Accelerated Model-based Mask Data Preparation and Other Computational Applications in Semiconductor Manufacturing
	9:40 - 10:05 AM	Ravi Kanjolia (EMD Performance Materials)	Atomic Layer Deposition Materials: Key Enablers for New Processes
	10:05 – 10:35 AM	BREAK	

Foundations for 3nm half-pitch patterning

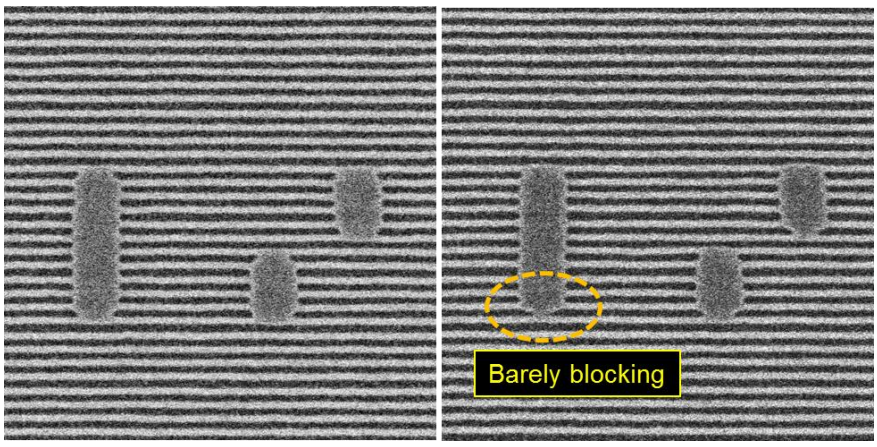
Richard Schenker
Components Research
Intel
Hillsboro, OR 97124

The adoption of patterning methods like Spacer Based Patterning (SBP) and (Litho-etch)^n or (LE)^n have broken the Rayleigh resolution (min half-pitch = k_1 □/NA) barrier for scaling. SBP, for example, has demonstrated the ability to generate one-dimension patterns with well below 10nm half-pitch. Scaling is now limited by the ability to accurately place edges of Vias, plugs, and cuts edges with respect to other existing layers and patterns. An example of this challenge is illustrated in the Figure below where a ~1/4 pitch shift in a plug pattern with respect to a 24nm pitch one-dimensional pattern results in an unwanted unblocked feature. The tightest pitch that can be utilized in practice is therefore limited and proportional to the Edge Placement Error (EPE) capability of the patterning system which can be simply stated as:

$$\text{Min Pitch} = p_1 * \text{EPE}$$

where p_1 is a process dependent variable.

Scaling to 3nm half-pitch requires significant improvements in both p_1 and EPE. The challenge is amplified because of the past success of scaling where now trillions of edges per wafer need to be well controlled. Etch, LER and OPC errors are consuming a larger portion of the total EPE budget and need innovative approaches to be consistent with 3nm half-pitch. Novel integrated approaches and materials can enable improvement in p_1 and will be discussed in the presentation.



Top-down of a 24nm pitch Via Chain test structure in hardmask with nominal (left) and ~ ¼ pitch programmed EPE (right).

Why we should escape 1D-centric e-beam lithography flow

Patrick Schiavone and Aselta team
Aselta Nanographics
7 Parvis Louis Néel; 38040 Grenoble, France

The number of curvilinear patterns used on the masks will increase drastically in the next generations of semiconductor devices. Inverse Lithography Technology (ILT), but also Silicon Photonics and many memory layouts make use of non-Manhattan patterns. This trend will be accelerated by the availability of multi electron beam writers that allow printing non-Manhattan patterns without any throughput penalty

On the other hand, the industry is still mostly living in a 1-dimensional, Manhattan world. A very illustrative example is that the specification and characterization of masks are almost exclusively based on 1-dimensional patterns like isolated or dense lines.

There are several difficulties to move forward caused by the limitations of the current technology toolbox to handle properly 2D features. For example, in-tool PEC has well known limitations for 2D patterns required by today's design rules. The most visible effect is scatter bars shortening that can reach several tens nanometers. The sizing algorithms of most existing data preparation software tools have been designed for Manhattan geometries; they start running out of steam when dealing with something else. On the characterization side, metrology tools still have a hard time measuring 2-dimensional patterns reliably and the usage of 2D metrics like contour is almost inexistent.

In this paper we will describe the state of the art of the technology and illustrate several of the limitations mentioned before. It will also be shown that the handling of 2-dimensional type of patterns is mandatory to successfully print next generation mask. Several examples covering correction, sizing and characterization will be given to demonstrate that the 2D challenge can be addressed efficiently.

GPU Accelerated Model-based Mask Data Preparation and Other Computational Applications in Semiconductor Manufacturing

Leo Pang
(D2S, Inc.)

Abstract not available at time of printing

Atomic Layer Deposition Materials: Key Enablers for New Processes

Ravi Kanjolia
EMD Performance Materials, Integrated Circuits
1429 Hilldale Avenue, Haverhill, MA 01845

Atomic Layer Processes, such as atomic layer deposition (ALD) have been adopted in the advanced generation semiconductor fabrication processes for nearly 10 years. The majority of these processes were limited to the deposition of thin metals, metal alloys, and metal oxide/nitride films in the FEOL and BEOL applications. Recently there has been an increased activity on the use of ALD in conformal multipatterning films like spacers and hard masks primarily due to the development of low temperature deposition processes including area selective growth. Selective ALD coupled with Atomic Layer Etching (ALE) process has further potential to extend the current lithographic processes for several nodes.

ALD technology offers atomic level control that is necessary to achieve superior conformality. Similarly, ALE has capability to remove films by atomic precision. The basic requirement of these techniques is the chemical and physical adsorption of the precursor materials in a self-limiting manner. The thickness control is achieved by repeating the precursor and coreactant pulse/purge cycles at a desired temperature. These precise processes pose enormous challenges in the design and development of ALD/ALE precursors with properties like volatility, stability, reactivity, and selectivity.

A brief review of the ALD/ALE technology followed by applications would lead in to a detailed discussion of the materials development process. Specific examples would be reviewed to illustrate the incorporation of specific properties in the ALD precursors. The influence of molecular design, surface deactivation, and deposition process parameters on selective area deposition would also be discussed.

Session 10

Presentation Schedule for
Thursday, November 10, 2016

Session Chairs
Mordy Rothschild
Marco Wieland

	Time	Presenter	Title
Session 10	10:35 – 11:00 AM	Grant Willson (Univ. of Texas at Austin)	Advances in DSA with high χ silicon containing block copolymers
	11:00 – 11:25 AM	Thomas Cecil (Synopsys)	Model Based Assist Features
	11:25 – 11:50 AM	Hakaru Mizoguchi (Gigaphoton)	
	11:50 – 12:15 PM	Eric Bouche (Ultratech)	Wafer shape process control in Foundry Lithography
	12:15 – 12:40 PM	Pieter Kruit (Delft / MAPPER)	From dose statistics to line edge roughness
	12:40 PM	End Session	

Advances in DSA with high χ silicon containing block copolymers

Grant Willson[1,2]; Christopher Ellison[2]; Michael Maher[1]; Gregory Blachut[2]; Austin Lane[2]; Yusuke Asano[1,3]; Natsuko Ito[1,3]; Yasunobu Someya[2,4]; Xiaomin Yang[5]; Roel Gronheid[6]; Dustin Janes[6] and Stephen Sirard[7].

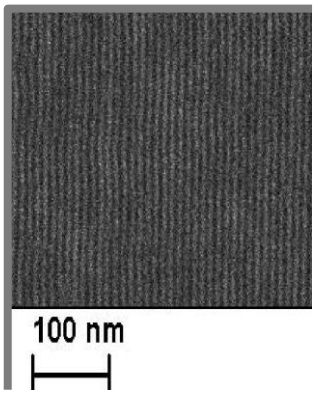
[1]Dept. of Chemistry, The University of Texas, Austin, Texas, USA; [2]McKetta Dept. of Chemical Engineering, The University of Texas, Austin, Texas, USA; [3]JSR Corp. Yokkaichi, Japan; [4]Nissan Chemical industries, Ltd.

Toyama, Japan; [5]Seagate Corp. Fremont, CA, USA; [6]IMEC Leuven, Belgium; [7]Lam Research Inc. Fremont, CA, USA;

A series of silicon containing block copolymers have been designed, synthesized and evaluated for use in high resolution directed self-assembly applications and progress has been made in understanding the directed assembly of the silicon containing polymers through studies at IMEC in Belgium and at Seagate in The USA. Several new monomers were synthesized and characterized for this study as were new block copolymers. The synthesis and characterization of the monomers and polymers will be presented. Most of these polymers were prepared by living anionic polymerization. The new polymers were studied in thin film form and neutral top coats, brushes and crosslinked bottom coat polymers were prepared and optimized using the previously described "island and hole method"[1]. The interaction parameters (⍰) for many of these polymers was measured using the small angle x-ray scattering methodology previously described[2]. The study has now produced materials that enable directed self-assembly of lamellae with 5nm lines and spaces as shown below. Etch processes have been developed that enable development of these structures to provide high aspect ratio patterns[3]. Focused ion beam milling experiments have provided thin cross sections of these patterns that were studied by transmission electron microscopy and electron energy loss spectroscopy to provide elemental mapping of the interaction between the block copolymer segments and the guiding structures. These studies have led to a new understanding of the importance of the interaction between the sidewall of the guiding patterns and the block copolymer lamellae[4]. Material and process design enable control of the selectivity of the reaction between the brush materials, the substrate and the patterned sidewall, which in turn, offers the opportunity to greatly reduce the resolution demands on the lithography used to produce the guide patterns.

References:

1. Maher, Michael J. ; Bates, Christopher M.; Blachut, Gregory; Sirard, Stephen; Self, Jeffrey L.; Carlson, Matthew C.; Dean, Leon M.; Cushen, Julia D.; et al. "Interfacial Design for Block Copolymer Thin Films," *Chemistry of Materials* **26(3)** 1471-1479 (2014)
2. Durand, William J.; Blachut, Gregory; Maher, Michael J.; Sirard, Stephen; Tein, Summer; Carlson, Matthew C.; Asano, Yusuke; Zhou, Sunshine X.; Lane, Austin P.; Bates, Ch "Design of high-χ block copolymers for lithography," *Journal of Polymer Science, Part A: Polymer Chemistry* **53(2)** 344-352 (2015)
3. Sirard, Stephen, Laurent Aza ; William Durand, Michael Maher, Kazunori Mori, Gregory Blachut, Dustin Janes, Yusuke Asano, Yasunobu Someya, Diane Hymes, David Graves, Chris Ellison and Grant Willson "Plasma etch of block copolymers for lithography," *Proc. SPIE* 9782, Advanced Etch Technology for Nanopatterning V, 97820K (March 23, 2016); doi:10.1117/12.2220305
4. Cushen, Julia D.; Lei Wan, Gregory Blachut, Michael J. Maher, Thomas R. Albrecht, Christopher J. Ellison, C. Grant Willson, and Ricardo Ruiz "Double-Patterned Sidewall Directed Self-Assembly and Pattern Transfer of Sub-10 nm PTMSS-b-PMOST.," *ACS applied materials & interfaces* **7(24)** 13476-13483 (2015)



Fifty Angstrom, 5nm lines and spaces in block copolymer assembled over guide lines . in imprint resist. The contrast has been enhanced by a brief exposure to oxygen reactive ion etching. This work was done in collaborration with Seagate Technologies and Lam Research

Model Based Assist Features

Thomas Cecil
Synopsys

The topic of model based assist features (MBAF) is one that has generated much discussion in the OPC community. In particular, there is debate over exactly what the definition of model based assist features is. In this talk I will review some of those discussions and related topics.

The first area I will cover is what many people typically think of when they hear the term MBAF. This includes complex all angle shapes which are generated from scratch during the mask synthesis run. These typically are generated from a pixel based mask representation and go through some post processing to create manufacturable mask shapes.

The next area I will cover is rule based assist features (RBAF). While these AFs are generated from a rule table, that rule table is often created through extensive modeling/simulation experiments and optimizations. Thus, often RBAF can be considered to be a version of MBAF. I will cover different algorithms which attempt to push the capability of RBAF as far as possible while still remaining rule based in the placement algorithm.

Finally, I will cover some model based optimizations that can be performed on AFs which have the goal of modifying their shapes and locations to improve various lithography metrics such as exposure latitude, depth of focus, MEEF, etc. I can refer to this in general as process variance (PV) optimization. This section does not discuss the creation of the initial AFs, but focuses more on their optimization after their initial placement. If this optimization is aggressive enough, it is difficult to distinguish the results of RBAF+PV optimization from the results of MBAF that are placed from scratch.

Throughout the talk I will mention other peripheral areas and dependencies of MBAF such as model calibration and prediction; mask rule requirements and enforcement; and mask complexity control and solution consistency.

Title to be announced

Hakaru Mizoguchi

Gigaphoton

Abstract not available at time of printing

Wafer shape process control in Foundry Lithography

Sean Lee, Albert Huang, CF Hua and Ming Sheng Wei ; Kennes Chen and Eric Bouche
UMC ; Ultratech

Wafer shape variability has become a significant detractor of high volume foundry manufacturing yield. Both in plane displacement (IPD, distortion) and topography residuals (planarization) have been correlated to advanced manufacturing lithography performance. The first directly impacts overlay, the second focus and critical dimension. The challenge that UMC and Ultratech Superfast have resolved is to translate these correlations into high volume foundry process control solutions. This presentation summarizes the process and results achieved over the past year at UMC advanced manufacturing site of Tainan, Taiwan.

Multiple authors have presented wafer shape characterization and the relation to the lithographic process. This helps the R&D of the latest foundry technologies. What has eluded many until this presentation is the development of robust metrology and statistical analysis to enable high volume manufacturing control. The UMC and Ultratech Superfast collaboration has focused into the robustness of advanced manufacturing process controls for both lithography overlay and focus.

This presentation will summarize the past year development and adoption of the Superfast wafer shape metrology into UMC's manufacturing lithographic process:

- The characterization of foundry CMOS microchip distortions and topography residuals
- The correlation of these metrics with the traditional 2D metrology and inspection solutions
- The characterization and optimization of the manufacturing processes for these metrics
- The deployment of high volume statistical control of these metrics for improved yield

It will also outline future projects and developments that are considered as extension of this successful collaboration, the challenges that UMC anticipate for its next generation foundry technology and what will be required from Ultratech Superfast to meet these challenges.

From dose statistics to line edge roughness.

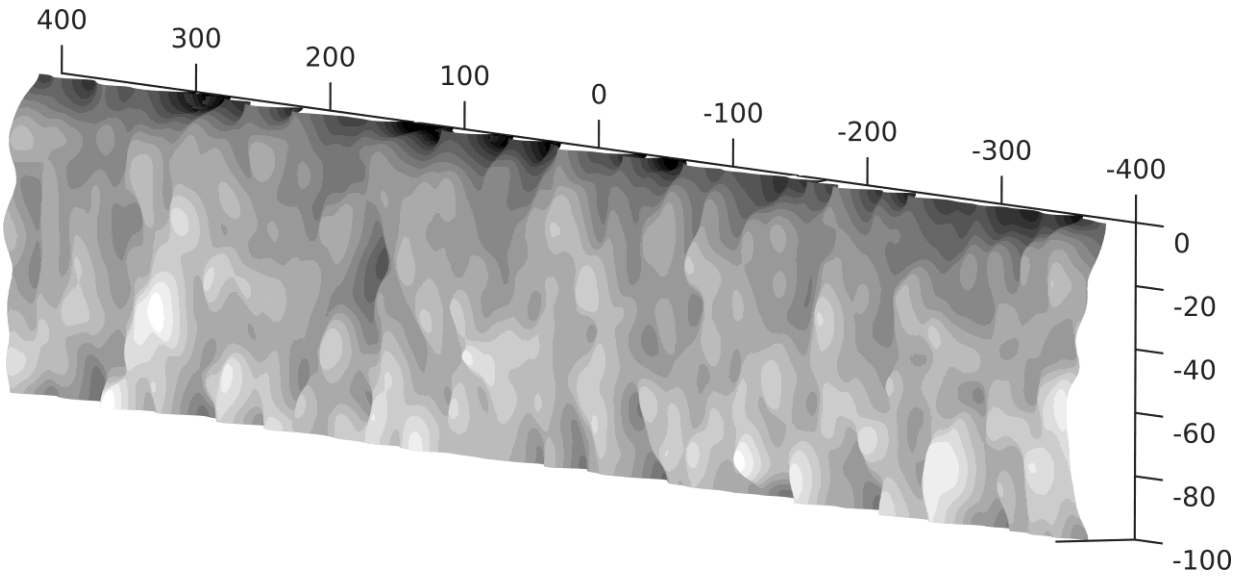
P. Kruit, T. Verduin, S.R. Lokhorst and C.W. Hagen.
Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands.

The throughput of a lithographic system is an important parameter. It is tempting to choose the most sensitive resist with the lowest possible illumination dose. In that limit, however, an increase of line edge roughness (LER) is observed. This increase of LER, primarily caused by fundamental quantum noise (shotnoise) effects, becomes the dominant mechanism in the formation of LER.

In this theoretical study, we first create a 3D resist pattern with side wall roughness and then image the pattern with a CD SEM, all in simulation. Our goal is to get a direct relation between input parameters such as resist properties or illumination profile and output parameters from typical measurements.

The initial distribution of photo acid generators (PAGs) is found by using a sophisticated simulator for electron-matter interaction. The distribution of PAGs is then used to determine the breaking of bonds in the resist by considering a diffusion like process in the post exposure baking (PEB) phase. We now set a threshold to determine the boundary between exposed and unexposed resist. In reality, there is also a development phase, which we so far have ignored in this study. We acknowledge that this is a simplified view of post lithographic processing. The exposed resist gives rise to a three dimensional feature which is then fed into our scanning electron microscopy (SEM) image simulator, which is the same Monte-Carlo simulator used for the lithographic exposure but now applied for the purpose of imaging. The line edge roughness in the resulting two dimensional top-down image is further processed using a power spectrum density analysis.

We find interesting ways of improving measured LER.



Session 11

Presentation Schedule for
Thursday, November 10, 2016

Session Chairs
Dave Pappas
Mark Somervell

	Time	Presenter	Title
Sessions 11	1:40 – 2:05 PM	Anthony Megrant (Google)	Reducing microfabrication-induced loss in superconducting devices
	2:05 – 2:30 PM	Naoya Hayashi (DNP)	
	2:30 – 2:55 PM	Alex Liddle (NIST)	Defectivity in Self-Assembled Structures
	2:55 – 3:25 PM	BREAK	

Session 12

Session Chair
Martha Sanchez

	Time	Presenter	Title
Session 12	3:25 – 3:50 PM	Shigeki Nojima (Toshiba)	Machine learning for DFM applications
	3:50 – 4:15 PM	Hamed Sadeghian (TNO)	
	4:15 – 4:40 PM	Laurent Pain (CEA – Leti)	Latest results of MAPPER technology toward its industrialization ramp up
	4:40 – 5:00 PM	Martha Sanchez	Closing Remarks and Announcements
	5:00 pm	End Session and Conference	

Reducing microfabrication-induced loss in superconducting devices

A. Megrant[1], A. Dunsworth[2], Z. Chen[2], C. Quintana[2], B. Chiaro[2], B. Campbell[2], R. Barends[1], B. Burkett[1], Y. Chen[1], A. Fowler[1], E. Jeffrey[1], J. Kelly[1], E. Lucero[1], J. Mutus[1], P. J.J. O'Malley[2], M. Neeley[1], C. Neill[2], P. Roushan[1], D. Sank[1], A. Vainsencher[1], J. Wenner[2], T. White[1], J. Martinis[1,2]

[1]Google Inc., Santa Barbara, CA 93117, USA
[2]Department of Physics, University of California, Santa Barbara, CA 93106, USA

A quantum computer will potentially solve far-reaching problems which are currently intractable on any classical computer. Superconducting qubits are a promising platform since their macroscopic size allows for easy control and coupling to other qubits. Many technological obstacles have prevented the realization of a quantum computer, the main obstacles being energy dissipation and decoherence, i.e. the loss of quantum information. Dissipation in these devices is currently dominated by coupling to material defects. These defects are present in the dielectrics used to fabricate these devices or introduced during fabrication. Previously we have decreased this source of dissipation in superconducting qubits by using simpler resonators as a testbed [1].

Superconducting qubits typically use submicron-scale Josephson junctions as their nonlinear elements.

These small junctions are fabricated using electron beam lithography and a Dolan bridge shadow mask [2]. The immediate area surrounding the junctions has recently been identified as a potential source of energy loss using finite element simulations. I will describe an experimental method to amplify and measure this source of dissipation using a novel resonator based approach, which we call 'Hydra' resonators. Using this method, we have measured a substantial amount of loss due to our Josephson junction fabrication process. We find that on silicon substrates this loss mechanism can lead to an order of magnitude higher dissipation.

I will describe a new fabrication process that mitigates this additional source of loss. The new process results in up to a factor of five improvement in coherence of Hydra resonators and superconducting qubits.

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Title to be announced

Naoya Hayashi

DNP

Abstract not available at time of printing

Defectivity in Self-Assembled Structures

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Self-assembling systems, such as DNA origami, hold great promise for the precise and reliable organization of nanostructures into higher-order functional units. However, when compared to semiconductor manufacturing, the defectivity levels are many orders of magnitude higher than those required for current device architectures. In this talk, we will discuss the origin of defects in these systems, and describe how defect levels might be expected to increase with increasing system size and complexity. We will also consider novel approaches to creating large structures, approaches that maintain molecularly precise addressability but reduce the probability of defect formation. One such approach, for instance, is to use indistinguishable units to assemble structures on longer length scales. Finally, we will speculate on the types of metrology tools that will be required to quantify the performance of self-assembling systems and assess the quality of the resulting structures.

Machine learning for DFM applications

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Design rules for layouts of advanced technology node keep shrinking to follow Moore's law. However, resolution limit is still limited by 193nm ArF immersion lithography system due to delay of next generation lithography tools. Various design for manufacturability techniques (DFM), such as resolution enhancement techniques (RET), optical proximity correction (OPC) and OPC verification have been proposed to fill the gap between the resolution limit and the layouts. For layouts of the advanced technology node, SRAFs which is one of RET techniques are necessary to keep resolution with sufficient lithography margin. There are mainly two methodologies to place SRAFs. One is rule-based and the other is model-based. Model-based SRAFs are generated based on a guide using a lithography simulation model. Model-based SRAFs can give better lithography margin than the rule-based method but computational time to place model-based SRAFs takes longer [1, 2]. Secondly, optical proximity correction (OPC) is applied to the layout. Model-based OPC (MBOPC) is mainly used for critical layers because of its accuracy supported by so-called compact model which enables lithography simulation for a full chip in a reasonable time [3, 4]. Model parameters in the compact model are optimized to minimize the difference between wafer CD of a set of test patterns and simulated CD of the patterns (calibration). Using the calibrated models, the initial layout is iteratively modified to match simulated image of the modified layout (OPCed layout) with the initial layout. Finally, the OPCed layout is verified by lithography simulation, which we call lithography compliance check (LCC). LCC checks if the OPCed layout has hotspots or not within a pre-specified process window [5]. In order to guarantee the process window, LCC conventionally uses several calibrated simulation models. Although simulation results by the models are accurate, the full chip simulation with plural simulation models is a computationally expensive step.

Due to the requirement of shorter time to market, these DFM steps are always under the pressure of shorter calculation time. In addition, accuracy is also required to prevent degradation of device performance and avoid unnecessary hotspots. To address these issues, we investigate DFM applications with machine learning. Machine learning can be represented as y=F(x). Y is output. X is input variables. F(x) is classification or regression function such as logistic regression, support vector machine and deep learning. For SRAF placement, the input X is features extracted from a layout and the output Y is SRAF positions. Parameters in the SRAF placement function are trained using layouts with SRAFs which are output of model based SRAFs. This machine learning based method can place SRAFs faster than the model-based method because the prediction of the SRAF positions using the F(x) can skip time consuming steps such as lithography simulation [6]. For a simulation model, the input is a layout pattern and the output is simulated CD of the input layout. Parameters in F(x) are trained using wafer CD of a set of test patterns. We apply deep learning as the F(x) for this calibration and get smaller differences between simulated CD and the wafer CD than the conventional method [7]. This model can be applied to OPC and we can get an accurate OPCed layout. Furthermore, relation between an OPCed layout and the initial layout can be trained as another F(x) to reach the OPCed layout faster. In order to balance between calculation time and accuracy, we propose a hybrid type. The latter machine learning function is applied to get a corrected layout and the corrected layout is used as the input of conventional OPC with the model calibrated on machine learning. First several iterations can be skipped and the latter OPC guarantees the accuracy on this hybrid type [8]. LCC, checking OPCed layout, has two purposes. One is to verify whether an initial has enough process window. The other is to check OPC recipes which are parameter set for OPC. In our presentation, LCC for the former purpose is discussed. Function of the relation between the initial layout and positions of hotspots is trained. The positions of hotspots are obtained not only by the conventional LCC but also by wafer inspection results. Calculation time can be reduced because OPC and LCC steps are described as one machine learning function [9]. In this presentation, we will discuss the detailed results, their pros and cons and potential applications using machine learning.

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Title to be announced

Hamed Sadeghian

TNO

Abstract not available at time of printing

Latest results of MAPPER technology toward its industrialization ramp up

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ABSTRACT

Massively parallel direct write E-Beam lithography technique is without any doubt an attractive alternative lithography technology. It offers a huge panel of competitive advantages, such as for example cost of ownership benefit, full writing flexibility opportunity and high-resolution potential [(1)]. On this field, MAPPER Lithography remains the leading company pushing the insertion of this technology solution up the industrial maturity. Through a joint partnership initiated in 2008 with MAPPER and in the frame of the open consortium IMAGINE, LETI works to demonstrate the capability of the MAPPER technology. These activities are focused on the insertion and the ramp-up of the pre-production platform FLX1200 installed with the LETI pilot line. This talk will detail the latest results of this technology toward its insertion and future adoption by the semi-conductor industry. A technical status will be presented. Finally, a discussion on the potential application fields addressed by this technology will be engaged to illustrate why and how the MAPPER technology can be quickly introduced into manufacturing.

L. Pain et al, «Direct write lithography : the global solution for R&D and manufacturing", C. R. Physique 7 (2006) 910-923

Poster Papers

Monday, June 22, 5:00 – 7:00 PM
Tuesday, June 23, 5:00 – 7:00 PM

Presenter	Title
Felix Holzner (SwissLitho AG)	Pattern transfer of 3D patterns and sub-15 nm half-pitch lines using a variety of hard masks for NanoFrazor lithography
Felix Holzner (SwissLitho AG)	3D NIL stamp fabrication on 200mm wafers with single nanometer resolution using NanoFrazor lithography
Norbert Koster (TNO)	Contamination Control for EUV lithography at TNO
S.R.J. Brueck (Univ. of New Mexico)	The CD/Wavelength Limits of Scatterometry
S.R.J. Brueck (Univ. of New Mexico)	GaN Tips for Atomic Force Microscopy/Scanning Tunneling Microscopy/Scanning Tunneling Lithography
Luigi Capodieci (KnotPrime, Inc.)	A Novel Data Analytics and Machine Learning Computational Framework for Design For Manufacturability
Jinseok Heo (Samsung)	Characteristics of OoB Distributions at the Wafer Level of EUV Lithography Tool
Kazuki Kasahara (Cornell Univ./JSR)	Nanoparticle photoresist development status for EUV lithography
Marco Wieland (Mapper)	MAPPER: High throughput maskless lithography
John S. Petersen (NanoTronix Inc.)	Exploring the potential of Multiphoton Laser Ablation Lithography (MP-LAL) as a reliable technique for sub-50 nm patterning
Mark Somervell (TEL)	Defect Reduction Results for Chemo-Epitaxy DSA Lines
Geert Vandenberghe (imec)	DSA as patterning option for memory and logic
J. L. Yoder (MIT Lincoln Labs)	Fabrication of High-Coherence Superconducting Qubits
Mary Ann Hockey (Brewer Science, Inc.)	Back End of the Line (BEOL) Strategy for Directed Self-Assembly
Tommy Oga (Gigaphoton Inc.)	The ArF Laser for the next generation cutting-edge ArFi lithography supporting green operations
Sergey Babin (aBeam Technologies, Inc.)	Accurate and fast analytical modeling of SEM images
Sergey Babin (aBeam Technologies, Inc.)	1.5 nm fabrication of test patterns for characterization of metrological systems
Dave Pappas (NIST)	Fabrication of Josephson junctions
Carlos Fonseca (TEL)	Multi-patterning
Yubing Guo (Kent State University)	Projection Photopatterning Molecular Orientations with Plasmonic Metamasks

Pattern transfer of 3D patterns and sub-15 nm half-pitch lines using a variety of hard masks for NanoFrazor lithography

Felix Holzner

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Thermal scanning probe lithography (t-SPL) has recently entered the lithography market as first true alternative to electron beam lithography (EBL). By now, the first dedicated t-SPL systems, called *NanoFrazor*, have been installed at research facilities in Europe, America, Asia and Australia by the company SwissLitho, a spinoff company of ETH Zurich.
Core of the technology - which has its origins at IBM Research and their Millipede project - is a heatable probe tip which is used for patterning and simultaneous inspection of complex nanostructures. The heated tip creates arbitrary high-resolution (<10 nm half-pitch) nanostructures by local decomposition and evaporation of resist materials. The patterning depth can be controlled with 1 nm accuracy, enabling patterning of 3D nanostructures in a single step.
Various pattern transfer methods based on reactive ion etching, lift-off, electroplating, ion beam etching have been demonstrated in combination with NanoFrazor lithography. This poster summarizes the processes that use a two, three or four layer hard mask stack for the pattern transfer processes. Results of 2D and 3D pattern transfer processes with a resolution < 20 nm half-pitch and line edge roughness below 3 nm (3σ) are shown for various materials. Examples for devices, including electrical nanowire transistors or spiral phase plates are shown.

3D NIL stamp fabrication on 200mm wafers with single nanometer resolution using NanoFrazor lithography

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Thermal scanning probe lithography (t-SPL) has recently entered the lithography market as first true alternative to electron beam lithography (EBL). By now, the first dedicated t-SPL systems, called *NanoFrazor*, have been installed at research facilities in Europe, America, Asia and Australia by the company SwissLitho, a spinoff company of ETH Zurich.
Core of the technology - which has its origins at IBM Research and their Millipede project - is a heatable probe tip which is used for patterning and simultaneous inspection of complex nanostructures. The heated tip creates arbitrary high-resolution (<10 nm half-pitch) nanostructures by local decomposition and evaporation of resist materials. The patterning depth can be controlled with 1 nm accuracy, enabling patterning of 3D nanostructures in a single step.
This poster shows examples of how such accurate 3D nanostructures structures have been used as stamps for nanoimprint lithography (NIL). NIL stamps have been fabricated in Si, Ni or soft and hard organic materials. Examples of the full NIL process using 200 mm wafers as stamps are demonstrated.
The patterning speed of t-SPL is comparable to that of high-resolution Gaussian shaped EBL, and a scan speed of 20 mm/s with a pixel rate of 500 kHz has been demonstrated. This throughput is still far too slow to cover the full area of a full 200 mm wafer on reasonable time scales. Various approaches towards increased throughput are shown, like parallelization using multiple tips and scan heads or mix&match lithography.

Contamination Control for EUV lithography at TNO

Norbert Koster, Edwin te Sligte, Jacques van der Donck, Diederik Maas, Herman Bekman

Abstract:
In this poster we will present the contamination control activities and infra structure at TNO International Centre for Contamination control (ICCC). Presently we are realizing EBL2; our second exposure facility for exposures of EUV optics, mask, pellicles and other EUV exposed components. The Ushio Sn fueled EUV source of EBL2 generates a spectrum close to the EUV scanner and can be used to study optics lifetime and surface contamination and degradation due to EUV irradiation under scanner conditions. Analysis can be done with in-situ XPS and ellipsometry and other methods like SEM-EDX, XTEM, XRR, XRD and EUVR. Besides EUV exposure we are also capable of exposing to high fluxes of hydrogen radicals and low energy ions to study interaction of radicals/ions with materials.
We are developing several metrology instruments to aid the industry in introducing EUV lithography in high volume manufacturing and clean production to enhance yield. A particle scanner that can detect 20nm particles in EUV blanks and an instrument that inspects a mask substrate within 2 min on backside particles is connected to a mask metrology platform. This platform will be used for developing ultraclean handling technology. Several types of microscopes, like SEM, AFM, and HIM, are used to classify the particle contamination. Dry cleaning using screened microwave and RF plasma systems and wet cleaning facilities are available for cleaning of sensitive surfaces and materials.

The CD/Wavelength Limits of Scatterometry

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Metrology is an essential adjunct to manufacturing. Ideally, metrology should be: real-time, so as not to limit throughput; non-destructive, and preferably non-contact so as not to interfere with the processing; should have sufficient resolution to monitor drifts and changes in the manufacturing line; and should be flexible in the sampling area and the numbers of samples. Optical metrology satisfies many of these constraints, but the issue for nanomanufacturing is the resolution when the optical wavelength is much larger than feature sizes (critical dimensions, CDs) and the periodicity of the structure. Scatterometry is an optical metrology based on diffraction from periodic structures that is well suited to the demands of nanomanufacturing of photonic and electronic components.[i-iii] It satisfies the demands of rapid, noncontact, on-line or at-line application, and has demonstrated resolution commensurate with advanced semiconductor nodes. Angular scatterometry was initially developed at the 180 nm node using a 633 nm wavelength source.[iv] Today it is being used at the 14 nm node. An advantage of angular scatterometry is that a broad spectrum model for the wavelength dependence of the various material optical properties is not required, often a difficulty particularly for deposited films whose properties can drift during manufacturing.

Nonetheless, the ultimate limits of scatterometry remain an important question We have explored this issue both with experiments and with modeling effort. Experimentally, we have investigated both high contrast (Al wire grid polarizers) and low contrast (photoresist) structures. Approximately 100-nm pitch, 50-nm *CD*, 200 nm high Al wire grid polarizers have been investigated for wavelength from 244- to 980-nm. At the longest wavelength the *CD*/λ ratio is about 20. Results at all wavelengths investigated are in good agreement and consistent with cross section SEM investigations. Eight parameters are necessary to fit the experiment: pitch, bottom width, top width, horizontal rounding, vertical rounding, Al height, fused silica undercut and Al_2O_3 thickness. Table I shows the fitting results..

Table I: Scatterometry fitting results of WGP with Al_2O_3

(nm) / λ(nm)	***P***	***BW***	***TW***	***Al***	***FS***	***HR***	***VR***	***var***
244	98.3±0.2	43.0±0.3	63.2±0.4	203±0.6	31.5±1.0	18.2±2.4	10.3±0.3	$8.80x10^{-3}$
405	97.2±0.4	49.4±0.2	58.6±0.4	208.3±0.9	22.9±2.2	25.8±1.2	14.8±0.6	$3.79x10^{-3}$
633	97.5±0.7	52.4±1.4	68.2±1.0	205.0±0.9	25.3±2.5	18.6±3.4	30.4±1.8	$5.85x10^{-3}$
982	97.5±1.0	49.4±1.0	69.2±0.4	203.1±5.4	14.4±7.4	20.6±10.0	8.7±2.8	$7.38x10^{-3}$
Aver	97.6	48.6	64.8	204.9	23.5	20.8	15.53	

Fig. 1 Shows the scatterometry experimental arrangement, Fig. 2 the cross section SEM results, Fig. 3 the parameterization of the model and Fig. 4 the fit between experiment and model. Fig.5 the limitation study for both metal grating and resist grating. Similar results are obtained for the low index contrast photoresist sample. Modeling has been used to evaluate the *CD*/λ limits of scatterometry for both of these 1D samples. Taking the experimentally observed signal:noise ratio and a broad angular scan. The high index contrast metal sample is more sensitive than the low index contrast photoresist.

This work is based upon work supported primarily by the National Science Foundation under Cooperative Agreement No. EEC-1160494.

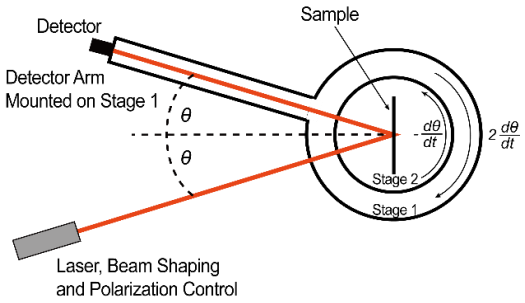

Fig. 1. Top view of experimental system. The sample is mounted on the rotation axis of two concentric rotation stages. The bottom stage moves to keep the reflected beam centered or detector as the angle of incidence is rotated.

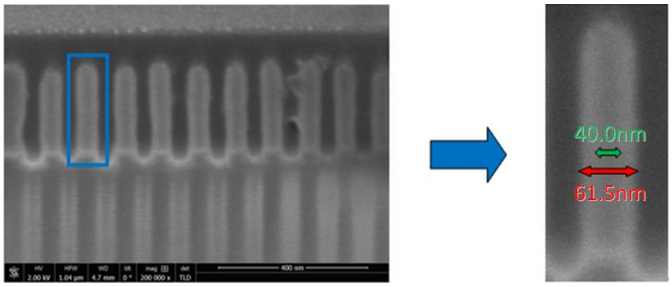

Fig. 2: Cross section SEM results.

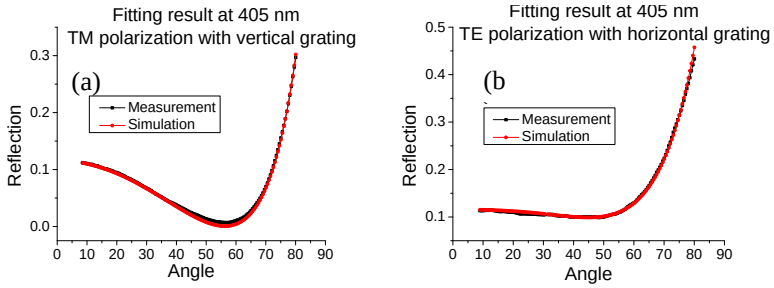

Fig. 4. Fitting results for 405 nm measurements: (a) TM polarization with vertical grating, (b) TE polarization with horizontal grating.

(a)

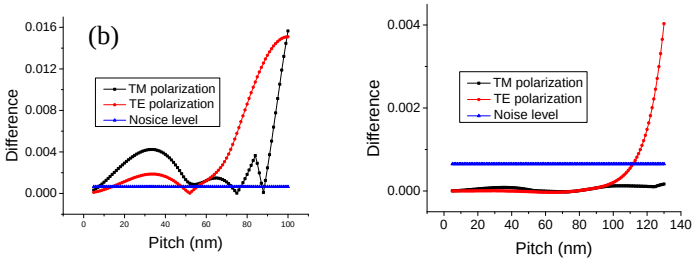

Fig. 5. Limitation study: Varying pitch, linewidth is half of pitch and grating height is equal to pitch. (a) Al grating on fused silica (b) Resist grating on polycarbonate. All calculations for a 405 nm scatterometry wavelength. The Al grating exhibits an oscillatory behavior with resolution to nm scales. The resist grating is already near the limit of resolution.

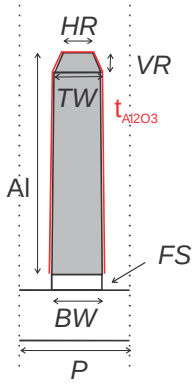

Fig. 3. Structure definition for WGP

GaN Tips for Atomic Force Microscopy/Scanning Tunneling Microscopy/Scanning Tunneling Lithography

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STM imaging and lithography both require sharp (~ 1 nm) tips and field-emission from the tip. AFM requires stiff tips with minimal sidewall roughness for probing 3D structures. Most often amorphous/polycrystalline metal tips are used, however these have high surface atom mobilities and are subject to reconfiguration. In contrast GaN has an exceptionally strong bond and is easily grown in a single crystal with a sharp termination (< 1 nm radius) defined by crystal planes. For both nanoscale epitaxial growth and top-down etching processes, the non-polar {1-1,0,0}M-planes of GaN provide almost perfect sidewalls with little surface roughness. GaN can be doped to provide the required conductivity for STM/STL and is a large bandgap semiconductor with optical emission that can be structurally tuned across the visible and near-UV. The sharp tips give rise to strong near-field enhancements that will be useful for near-field probes.

We have developed selective-area epitaxial growth and doping techniques for GaN nanowires. and the technology for mounting the nanowires on Si (AFM tips) and on metal wires (STM/STL). Fig. 1 shows the as-grown tips. In Fig. 2a the end of the sharpened metal wire was flattened with a focused ion beam (FIB) and a ~ 0.5 □m diameter GaN nanowire was welded to form the STM tip. Similarly, as shown in Fig. 2b, a GaN single crystal NW was attached to a tipless Si cantilever to be used in non-contact mode for imaging and as a near field probe. The 6-fold facet symmetry of the GaN M-planes is evident along the vertical sidewalls; the top of the tip can be either flat or pointed depending on the growth conditions. Tip radii of less than 1 nm have been observed in TEM studies. The imaging and the lithographic properties of the final tip have been investigated. Fig. 3 is a negative sample bias STM image of an H-passivated Si surface showing the 2×1 dimer reconstruction. The white line was written using a high current and a positive sample bias. Work is underway to study the durability of these tips. Moreover we are also working on AFM tip with smaller diameter for improved high aspect ratio measurements on steep sidewalls. In future work, we expect to be able to grow the tips directly on Si pedestals, greatly simplifying the fabrication process.

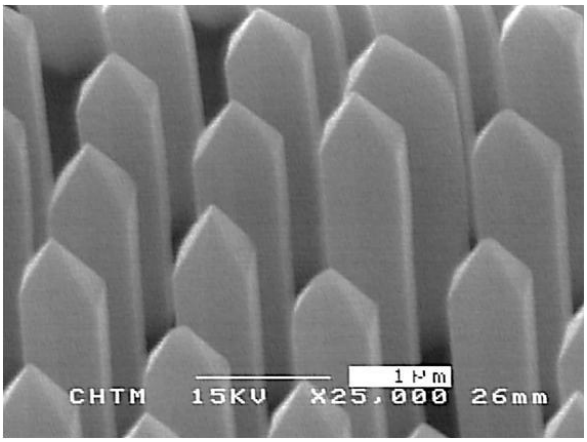

Fig. 1: Array of "as-grown" GaN tips using selective area growth.

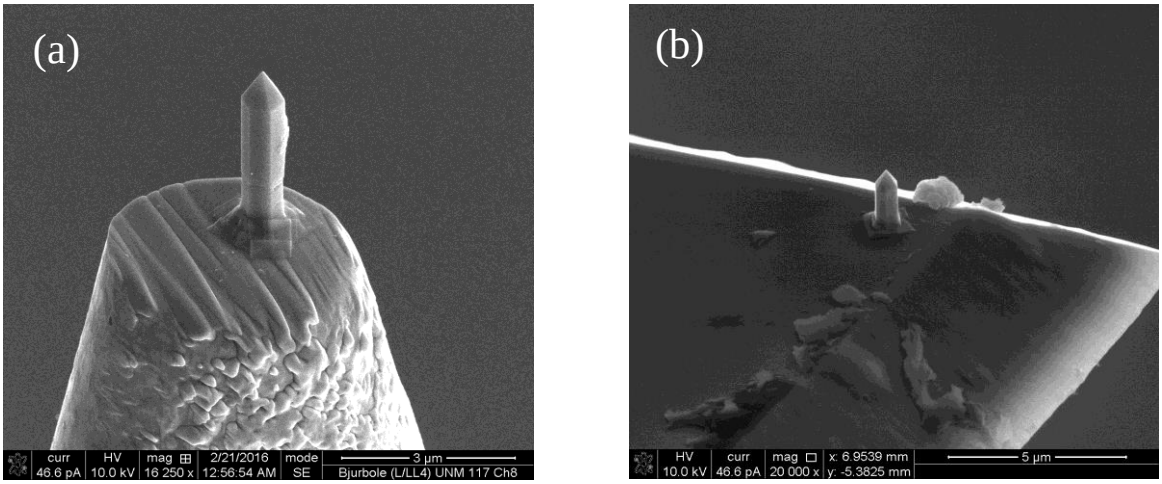

Fig. 2: GaN nanowire mounted (a) on the end of a PtIr wire for STM probe, and (b) on a Si tipless cantilever for AFM and NSOM applications.

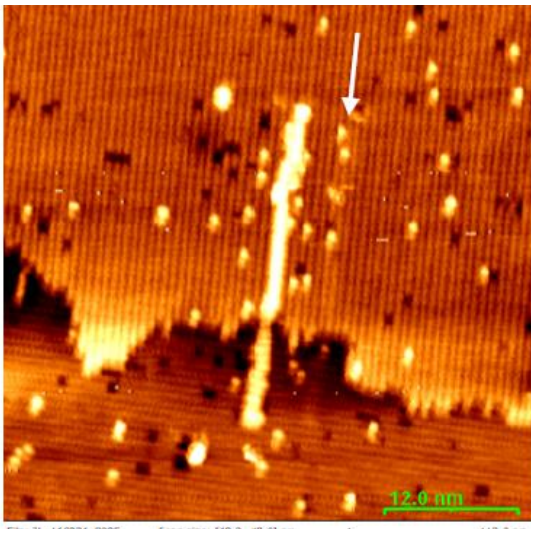

Fig. 3: ~ 1 nm wide H-deprotection line written on reconstructured Si(211) surface.

A Novel Data Analytics and Machine Learning Computational Framework for Design For Manufacturability

Luigi Capodieci
KnotPrime, Inc.

Starting from a synthetic survey of the state-of-the-art and ongoing developments in Data Analytics and Machine Learning, this work offers a perspective on the functional interactions and *data information flows* for IC Design-to-Manufacturing, and highlights risks and opportunities arising from the introduction of big-data (algorithmic) analytics and machine learning technologies, in response to the current challenges of advanced (end-of-Moore) IC nodes and semiconductor industry consolidation.

A quantitative definition of *physical design space coverage* is proposed, as the unifying abstraction available for all components of the Design-to-Manufacturing flow, allowing for the construction of a computational framework where (big) Data Analytics and Machine Learning methodologies and tools can be successfully applied.

The juxtaposition of Design-Technology-Co-Optimization (DTCO) with the novel paradigm of DFM-as-Search and their necessary integration in the DFM computational toolkit, clearly exemplify how the very advanced IC nodes (10, 7 and 5nm) can not only benefit from, but definitely require the adoption of a new class of correlation extraction algorithms for heterogeneous data sets.

Characteristics of OoB Distributions at the Wafer Level of EUV Lithography Tool.

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Keywords: EUV, OoB DUV, Lithography, NXE3100

Although the progress has been greatly delayed, extreme ultraviolet (EUV) lithography is now considered to be a viable or possibly mandatory solution in economic terms for patterning of the next generation semiconductor. However, excluding the source power itself, many other technical issues must be overcome before EUV lithography can be adopted in mass production processes. To improve and to understand the performance of EUV source which can impact on CDU, the novel dose measurement at the wafer-level was developed using the enhanced energy sensitivity by resist contrast (EESRC) method [1]. The EESRC method uses captured images from the conventional macro inspection system rather than resist thickness measurements. This metrology system is commonly used for the novel process and equipment monitoring [2-3]. The EESRC method is based on the phenomenon where, under chemical amplification, the thickness of a photoresist becomes extremely sensitive to the applied dose and the resist thickness changes can be detected based on the changes in the color intensity of the captured image. As EESRC can make the energy distribution map including the unexpected light, so-called, out of band DUV (OoB DUV) at the wafer-level, this method can provide the details about the dose performance of EUV lithography tool. In this paper, using the newly introduced measurement, the EESRC method, how the OoB DUV in the energy distribution map can be analyzed and how much improvement can be achieved by the conventional suppression technologies.

Figure 1 shows the normalized energy distribution in the high-end EUV scanner (ASML NXE 3300) by using EESRC method. The noticeable fingerprint shown in these figures is noticed as bright bands that indicate abrupt dose jumps at the edge of the fields, with a range of approximately 500 um. This band-like CD variation under an exposure field is a well-known EUV-specific phenomenon that is associated with image border or black border reflections of the in band EUV and OoB DUV light.

There are few technologies have been introduced to minimize this effect during the exposure. Outgassing and out of band protection layer (OBPL) is the one of the famous technologies to suppress the black border impact by coating the additional material to reduce the OoB DUV on the photo-resist. The other approach to improve the uniformity of energy distribution is to minimize the reflection of DUV at the black boarder of reticle. Although these technologies are applied, it is very difficult to quantify how much OoB DUV is suppressed. The EESRC method is very beneficial metrology to understand the OoB DUV distribution at the wafer- level quantitatively such as figure 2 by introducing the equivalent EUV intensity by OoB DUV experienced in the EUV photoresist, although it cannot make the spectrum of OoB DUV.

Through the detailed experimental results and analysis, we introduce how much OoB DUV can be removed by few suppression technologies mentioned before. In addition, we can estimate the remains of OoB DUV should be mitigated in the EUV scanner for the mass production.

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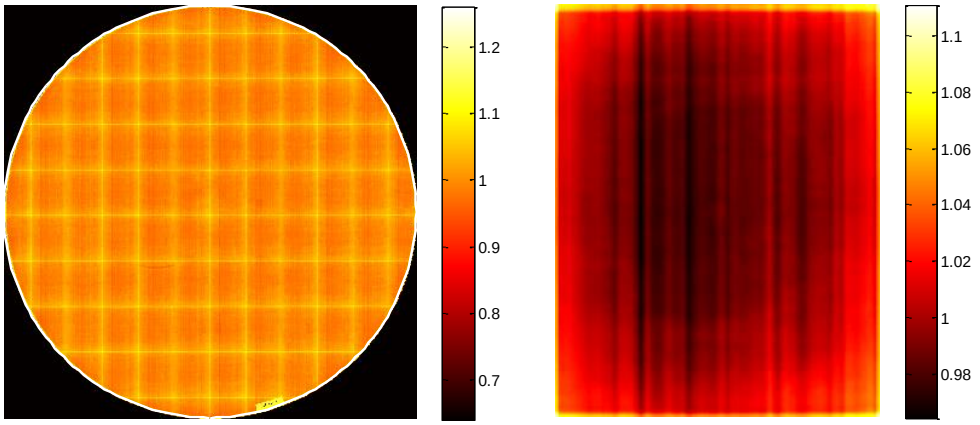

Figure 1. Energy distribution map based on EESRC: (a) in-wafer energy distribution map, (b) in-field energy distribution map.

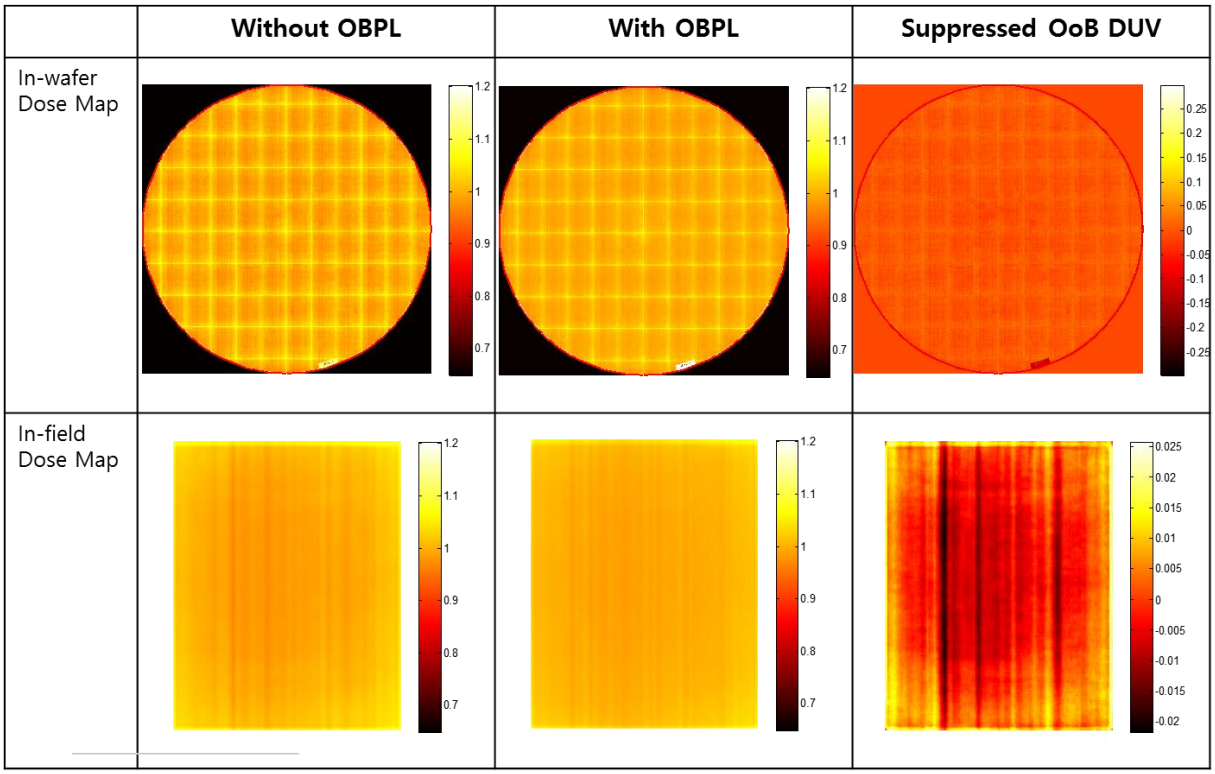

Figure 2. Analysis of the suppressed OoB DUV effect by OBPL using EESRC (Normalized energy distribution)

Nanoparticle photoresist development status for EUV lithography

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EUV lithography is a promising candidate for next generation lithography. For high volume manufacturing of semiconductor devices, significant improvement of resolution and sensitivity is required for EUV resists. The performance requirement for EUV resists requires the development of new resist platforms.

Cornell University has intensively studied metal oxide NP (nanoparticle photoresist) for EUV lithography applications. ZrOx NPs with PAG enabling sub 30nm line negative tone patterns at an EUV dose below 5 mJ/cm^2, show one of the best EUV sensitivity results ever reported. In this presentation, recent progress in metal oxide nanoparticle resists will be discussed. A patterning resolution improvement study with ZrOx NPs and studies of a new metal core will be mainly described.

For the patterning resolution improvement, scum improvement at dense fine pattern is big challenge for ZrOx NPs. Additive, ligand and process optimization studies including development condition study have been carried out recently.

Regarding the new metal core study, new metal elements have been applied to nanoparticle resists in terms of high EUV absorbance for better lithography performance. Especially new ZnOx NP shows good resolution compared to ZrOx NPs. E-beam and EUV exposure experiment results will be discussed.

MAPPER: High throughput maskless lithography

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ABSTRACT

Mapper Lithography has introduced its first product, the FLX–1200, which is installed at CEA-Leti in Grenoble (France). This is a mask less lithography system, based on massively parallel electron-beam writing with high-speed optical data transport for switching the electron beams. This FLX platform is initially targeted for 1 wph performance for 28 nm technology nodes, but can also be used for less demanding imaging. The electron source currently integrated is capable of scaling to 10 wph at the same resolution performance, which will be implemented by gradually upgrading the illumination optics. The system has an optical alignment system enabling mix-and-match with optical 193 nm immersion systems using standard NVSM marks. The tool at CEA-Leti is in-line with a Sokudo Duo clean track. Mapper Lithography and CEA-Leti are working in collaboration to develop turnkey solution for specific applications.

On this poster we will present the basic working principles and the key performance data of the FLX-1200 tool such as imaging performance, throughput, uptime and initial overlay data

Figure 1, FLX-1200 tool installed at CEA-Leti

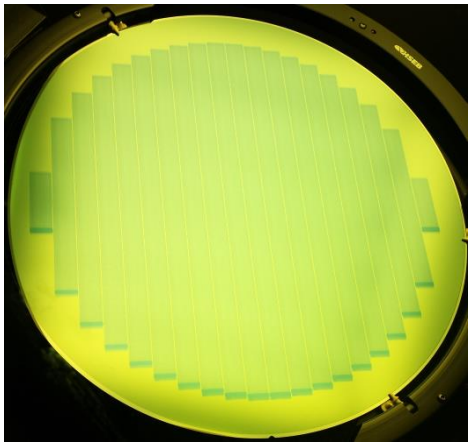

Figure 2, Wafer exposed in less than 1 hour

Exploring the potential of Multiphoton Laser Ablation Lithography (MP-LAL) as a reliable technique for sub-50 nm patterning

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Presented by John S. Petersen, Petersen Advanced Lithography, Inc.
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In this work, direct-write, high-resolution multiphoton photolithography using doped random methacrylic co-polymer thin films is demonstrated, using a continuous wave ultraviolet (UV) 375 nm diode laser source. The random copolymers are specifically designed for enhancing resolution and addressing issues arising from laser ablation processes, such as the berm-formation around the created holes in the film, which can be accessed by tuning the polymeric material properties including Tg, surface adhesion etc. The methacrylic copolymer is composed of monomers, each of them especially selected to improve individual properties. The material formulations comprise perylene molecules absorbing at the exposure wavelength where the polymeric matrix is transparent. It was found that if the radiation intensity exceeds a certain threshold, the perylene molecules transfer the absorbed light energy to the acrylate polymer matrix leading to polymer degradation and ablation of the exposed areas. The non-linear nature of the light absorption and energy transfer processes resulted in the creation of holes with critical dimensions well below the used wavelength reaching the sub 50 nm domain. Arrays of holes having various dimensions were fabricated in the laser ablation experiments using a direct-write laser system developed specifically for the purposes of this project.

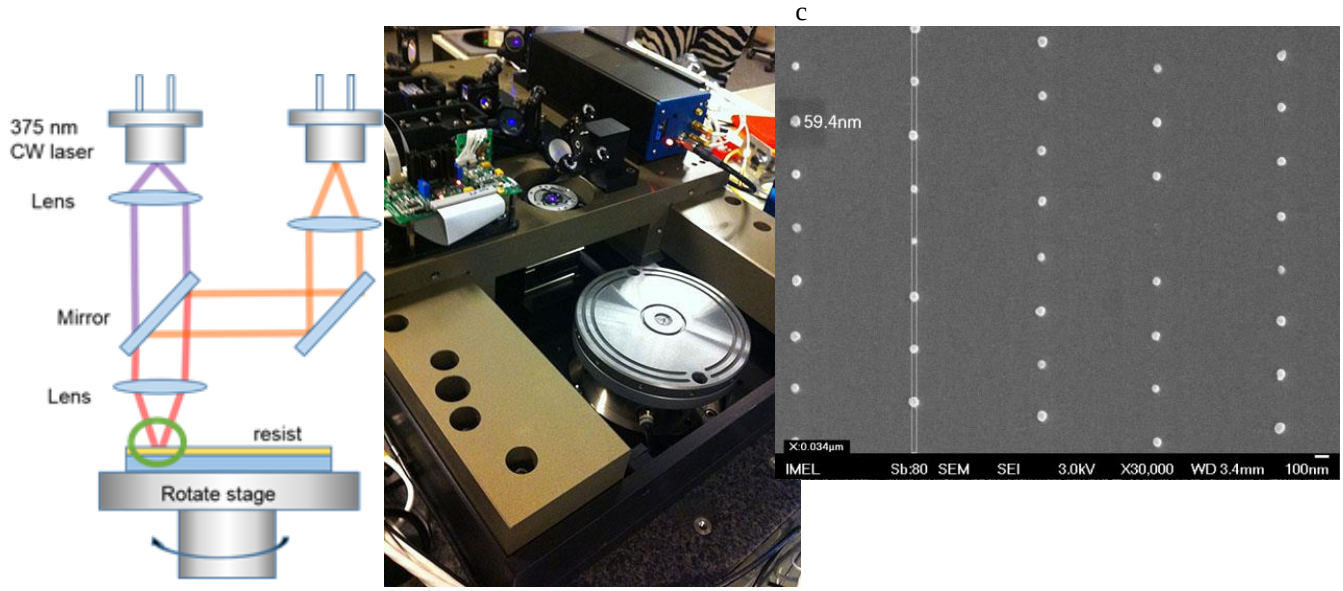

Figure 2: a) Conceptual Setup, b) Linear-Rotary Airbearing Close-up and c). Polymer 5 thin film written by LBR. Ni pillars with various dimensions range from 30 to 60 nm.

Defect Reduction Results for Chemo-Epitaxy DSA Lines

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Directed self-assembly (DSA) is one of the candidates for next generation lithography. Over the past few years, block copolymers forming cylindrical and lamellar structures have been investigated for use in contact hole and lines/space patterning, respectively. Tokyo Electron Limited (TEL is a registered trademark or a trademark of Tokyo Electron Limited in Japan and /or other countries) has reported patterning results, process advantages, and challenges associated with each apporach[1-5].

One of the biggest challenges in applying DSA technology to semiconductor manufacturing is pattern defectivity. For line/space patterns, dislocations and bridged lines are often observed. Numerous causes have been suggested as the primary source of the defects including substrate particles, guide pattern mismatching, and issues with various DSA chemicals. Furthermore, doing detailed, defect partitions of the individual steps is difficult because such a large number of steps are used to create the chemical template. Thus in this report, simulation methods are used to study typical defect types, and simulated defect shapes are compared with experimentally observed defects. Using these simulation methods, potential root causes of defectivity can be explored, and promising simulation results can drive real-world solutions for reducing on-wafer defectivity.

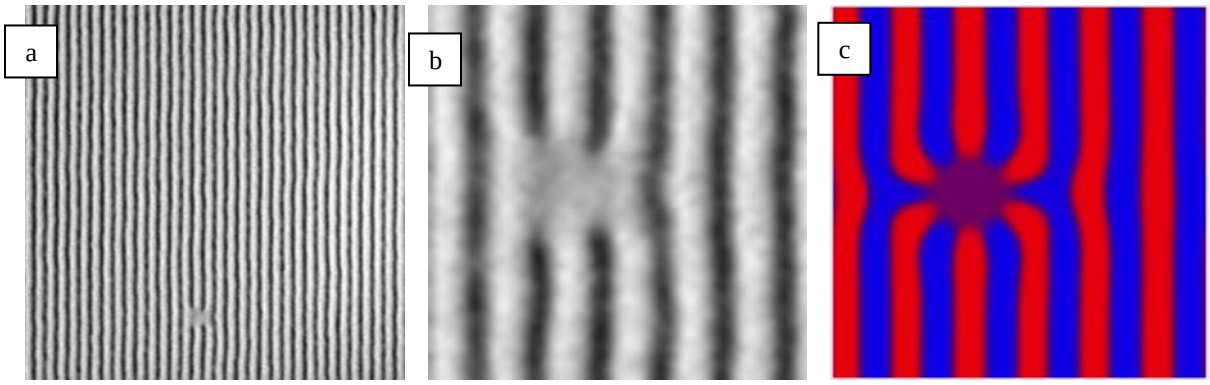

Figure 1: a,b) Typical bridge defect on DSA patterns, c) Top view of the 3D simulation result.

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DSA as patterning option for memory and logic

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Directed self-assembly (DSA) has been considered for patterning in IC manufacturing for several years, but has yet to make it into production. The main merits of DSA as patterning technique lie in its potentials for cost reduction, CD uniformity improvement, and pitch scaling. Challenges on the other hand for DSA as manufacturing technique are seen in process defectivity, material quality control, and its impact on design rules.

In this poster three use cases for DSA will be explored and assessed in terms of their readiness:

1) DSA for line/space patterning as SAQP replacement in FEOL or BEOL
2) DSA for via patterning at the N7 and N5 logic nodes
3) DSA for DRAM storage node patterning

For each of the techniques, readiness will be determined in terms of the merits and challenges of DSA and a comparison to the most likely patterning competitor of DSA will be made.

Fabrication of High-Coherence Superconducting Qubits

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Superconducting qubits are a promising candidate for the fundamental logic element of a quantum information processor. When cooled to milliKelvin temperatures, these lithographically-defined electronic circuits behave as "artificial atoms," featuring an anharmonic spectrum of quantized energy levels arising from the non-linear inductance of Josephson tunnel junctions. Over the past 15 years, advances in the fabrication, materials, and design of superconducting qubits have led to significant improvements in their coherence time [1], which is a key metric to characterize their quantum mechanical performance. Such high-coherence superconducting qubits are now being engineered for quantum annealing and gate-based computing applications. Here we will describe our work at MIT Lincoln Laboratory to fabricate high-coherence superconducting qubits [2]. We will discuss our process flows, which include patterning by photolithography and electron beam lithography to fabricate shadow-evaporated aluminum Josephson junctions and high-quality- factor circuit elements (e.g., capacitors, resonators). For reference, in Figures 1 and 2 we include schematics of our baseline process flow and scanning electron micrographs of our high-coherence capacitively-shunted flux qubits, respectively. We also will highlight aspects of our work related to the materials growth and characterization of high-quality superconducting titanium nitride and aluminum films, as well as the development of 3D-integrated superconducting circuits.

The Lincoln Laboratory portion of this work was sponsored by the Assistant Secretary of Defense for Research & Engineering under Air Force Contract number FA8721-05-C-0002. Opinions, interpretations, conclusions and recommendations are those of the author and are not necessarily endorsed by the United States Government.

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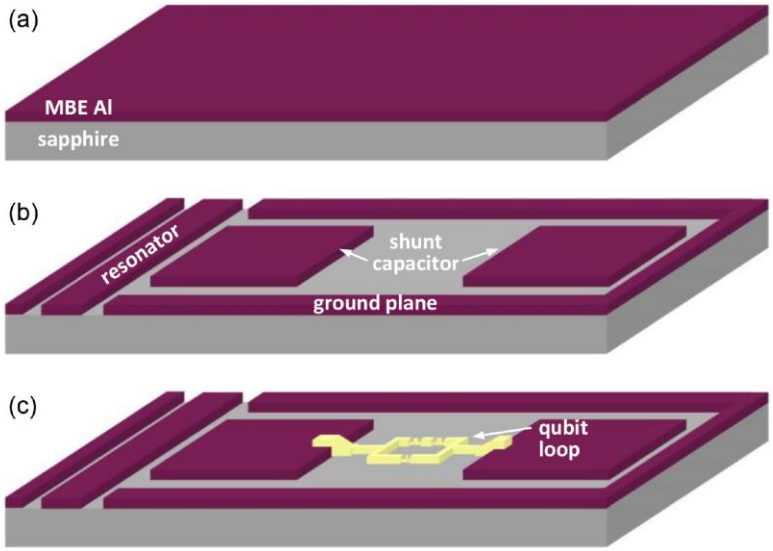

Figure 4: Process flow schematics of key steps for fabrication of superconducting capacitively-shunted flux qubits. (a) Preparation of MBE aluminum (red) on outgassed C-plane sapphire substrates (gray). (b) Patterning of the MBE aluminum into the shunt capacitor (representative square shunt capacitor geometry is shown), resonator center line, and surrounding ground plane. (c) Patterning of the aluminum qubit loop (yellow), which contains three aluminum Josephson junctions. The loop contacts the shunt capacitor as illustrated.

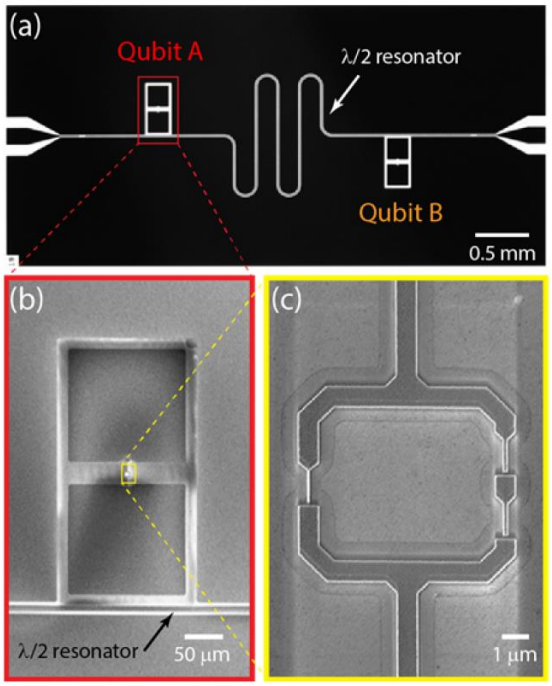

Figure 2: Scanning electron micrographs of superconducting capacitively-shunted flux qubits. (a) Optical micrograph of the 2.5 x 5.0 mm^2 chip, aluminum (black) on sapphire substrate (white, where the aluminum has been etched away), featuring two qubits (A and B) and a λ/2 coplanar waveguide resonator. (b) SEM image of the shunt capacitor for qubit A. Each square plate of the capacitor is 200 × 200 μm^2. The lower plate capacitively couples the qubit to the λ/2 resonator. (c) Magnified view of the shadow-evaporated qubit loop and its three Josephson junctions.

Back End of the Line (BEOL) Strategy for Directed Self-Assembly

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Complimentary random brush layers tuned for surface energy properties consistent with block co-polymer (BCP) capability has been developed specifically for guides with metal containing compositions. BSI high χ BCP can be customized to work efficiently with values from 16-30 nm L_0. This approach enables identical compositional materials to further shrink pitches to below 18 nm as design rules necessitate without changes to the composition of the BCP. No top-coat or solvent anneal is required with our high χ formulations. The significant benefit of is that our BCPs combined with customized random brush layers are ideal for BEOL process requirements for grafting to metal surfaces successfully.

The ArF Laser for the next generation cutting-edge ArFi lithography supporting green operations

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ArF immersion lithography used for 10nm Node and beyond has been expected as the promising technology to meet tighter cutting-edge device requirements. In general, the Light-source requires supporting less process margin for the leading node by precise spectrum control and stable dose energy. In the other hand, the Light-source would demand more productivity and more cost effective solution including support green operations. Especially, the dependence on rare gases, such as neon and helium, is becoming a critical issue for HVM process. These two aspects could be controversial situation in terms of Light-source development and engineering activity. Gigaphoton has been working on the solutions to compromise these aspects by implementing the material engineering and hardware design engineering with optimizing the gas management. Hence, the new ArF excimer laser, GT64A has been developed to cope with the reduction of operational costs, the prevention against rare resource shortage and the improvement of process yield while ArFi runs for the most critical lithography layer processes.

Based on the field-proven injection-lock twin-chamber platform, GT64A has advantages in efficiency and stability and this leads to cost-effective green operations while improving performance. The first is the reduction of gas usage. One is neon. More than 96% of the gas used in the lasers is neon. Another gas that requires attention is helium. Recently the unstable supply and the shortage supply of neon and helium became a serious worldwide issue. To cope with this situation, Gigaphoton is developing lasers that support reduction of neon usage and completely helium-free operations. The injection-lock twin-chamber platform has capability to execute a new advanced gas control algorithm in which parameters, such as input power and gas pressure are closely monitored during operations and fed back to the injection/exhaust gas controller system. By introducing this new gas control to twin-chamber platform, the laser gas consumption can be reduced by up to 50%. Furthermore, Gigaphoton aims to challenge of Neon free operation introducing Gas recycle system while the lasers maintains without performance loss or productivity loss which provides Eco-friendly solution to the chipmaker.

In addition newly designed Line Narrowing Module can realize completely helium free operation. Even without helium gas purge, the spectral bandwidth becomes equal to that of the conventional helium purge. Narrower spectral bandwidth enhances image contrast and therefore enables the excellent CD control for device manufacturers.

These technologies and the detailed properties of GT64A will be discussed in detail.

Summary;

The new ArF excimer laser, GT64A has been developed to cope with the reduction of operational costs, the prevention against rare resource shortage and the improvement of device yield integrated to cutting-edge ArFi lithography tool used for 10nm and beyond technology node.

GT64A has advantages in both performance and eco-friendly operation. The consumption of rare gases such as neon are reduced to a half by the combination of injection-lock twin-chamber platform and the advanced gas control algorithms, and completely helium free operation can be realized. The improvement in spectral bandwidth stability increase image contrast and contribute to the further reduction of CD variation.

Accurate and fast analytical modeling of SEM images

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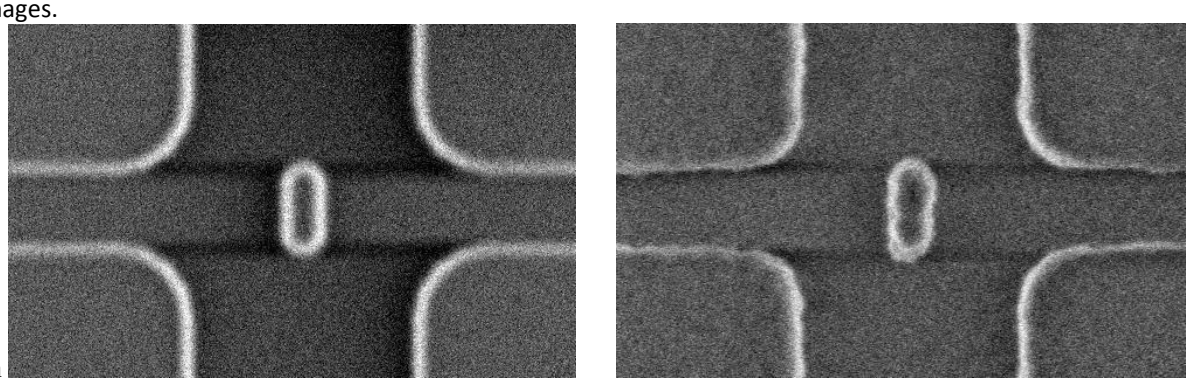
Scanning electron microscopy is an indispensable part of semiconductor manufacturing, especially in CD metrology and defect inspection and review. Monte Carlo simulators of SEM image formation provide highly accurate results by modeling the scattering of each electron, including secondary electrons. Advanced simulators include electron scattering of primary and secondary electrons, as well as the detectors, electromagnetic fields and charging. However, the high accuracy comes at the cost of long simulation times. During the last few years, a few extremely simple models of SEM, or emulators, have been developed. While the modeled images looks roughly like SEM images, the capabilities of such emulators are extremely limited and, in fact, misleading.

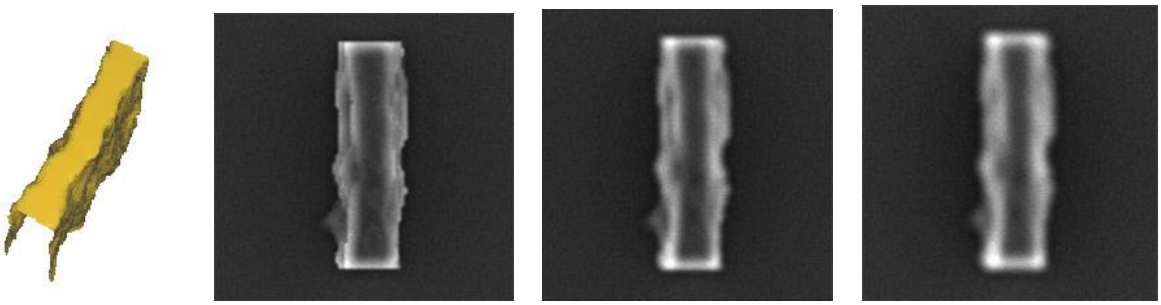
aSEM uses an analytical model of the SEM which takes into account the major effects of electron scattering and image formation in the SEM. The beam voltage and size, scanning parameters of the beam, physical properties of the materials and 3D shapes of features are considered. The geometry and properties of both the backscattering and secondary electron detectors are modeled. Extracting or suppressing electrical fields over the sample is also taken into account. Finally, sample charging is also considered. In this way, the accuracy of the analytical model approaches the accuracy of Monte Carlo simulators.

This complex modeling makes the simulation results accurate. In this way, this is a true analytical model of an SEM, not just an emulator. On the other hand, simulation time is short, typically within one minute - a huge improvement compared to Monte Carlo simulators that take multiple hours. Simulations of a variety of test samples at variable beam settings were performed, especially images with charging. These examples of simulations are discussed and compared to SEM images.



a b

Figure 1. a) Simulated and b) experimental SEM images of resist pattern. Charging is well noticeable. The main details of the image were reproduced in the simulation, including brightness enhancement at vertical edges different from that at horizontal edges and shadows due to charging. The simulation time was about one minute.



a b c d

Figure 2. SEM images of an individual 22 nm resist line from HyperLith (a) were simulated at electron beam sizes b) 0.5 nm, c) 2 nm and d) 4 nm.

1.5 nm fabrication of test patterns for characterization of metrological systems

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100 words:

To characterize metrology systems, test patterns that are one order of magnitude smaller than the measured features are required. Test patterns with linewidths down to 1.5 nm were designed and fabricated. The test pattern contains hundreds of alternating lines of silicon and tungsten silicide. The test sample was designed in such a way that the distribution of the linewidths appears to be random at any location and magnification. This pseudo-random test pattern is used to characterize metrological equipment in their entire dynamic range.

Abstract

The semiconductor industry is moving toward a half-pitch of 11 nm and 7 nm. The required metrology equipment should be at least one order of magnitude more accurate than that. The characterization of metrology systems requires test patterns that are one order of magnitude smaller than the measured features. Test patterns with linewidths down to 1.5 nm were fabricated. The test patterns contain alternating lines of silicon and tungsten silicide that provide good contrast in images. The size of the test sample was approximately 6x6 microns and involved hundreds of lines, each according to its designed width.

The test sample was designed in such a way that the distribution of linewidths appears to be random at any location and any magnification. This pseudo-random test pattern is used to characterize metrological equipment. The power spectral density of such a test pattern is inherently flat, down to the minimum size of lines. Metrology systems add a cut-off of the spectra at high frequencies; the shape of the cut-off characterizes the system in its entire dynamic range, describing the loss of sensitivity as the linewidth decreases. This method is widely used to characterize optical systems, and has allowed optical systems to be perfected down to their diffraction limit. There were attempts to use the spectral method to characterize nanometrology systems such as SEMs, but the absence of natural samples with known spatial frequencies was a common problem. The system characterization includes the imaging of a pseudo-random test sample and image analysis by a developed software to automatically extract the power spectral density and the contrast transfer function of the nano-imaging system.

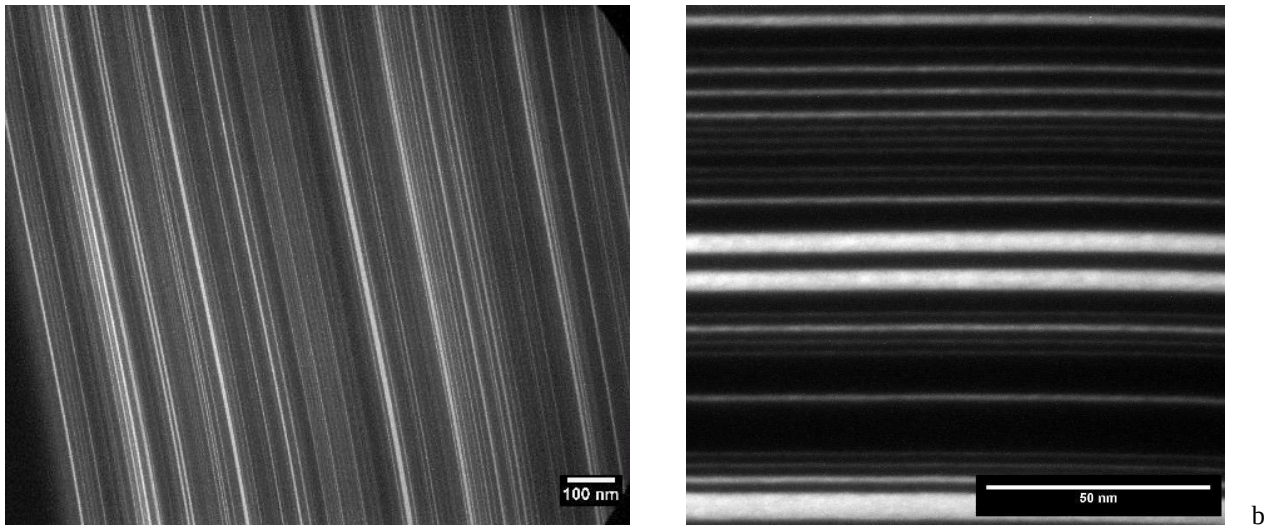

Figure 1. TEM images of the test pattern with linewidths down to 1.5 nm. The width of the lines was designed to form a pseudo-random test pattern; the pattern is used to characterize metrological instrumentation. The scale bars on the image (a) is 100 nm, on the image (b) is 50 nm.

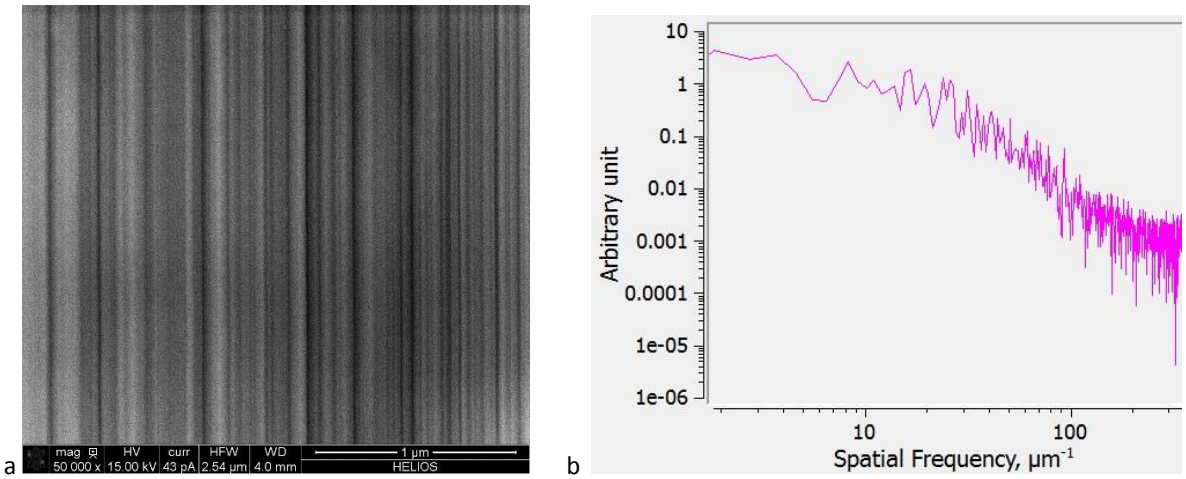

Figure 2. a) SEM image of a test sample, b) power spectral density of the SEM.

Fabrication of Josephson junctions

Dave Pappas

(NIST)

Abstract not available at time of printing

Multi-patterning

Carlos Fonseca
(TEL)

Abstract not available at time of printing

Projection Photopatterning Molecular Orientations with Plasmonic Metamasks

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Designable and complex molecular orientations are the essence of many emerging applications of liquid crystals (LC), such as programmable origami based on LC elastomers, diffractive gratings and Pancharatnam geometric lenses. Existing techniques to realize complex molecular orientations are all serial processes, relying on pixel-by-pixel patterning, and thus not suitable for scaling up manufacturing. We present a novel technology to pattern molecular orientations by using engineered plasmonic metamasks (PMMs). In contrast to photomasks used in traditional lithography where only intensity patterns are used, the PMMs generate spatially variant patterns of both light intensity and polarization directions. This new parallel photo patterning processes features high throughput, high resolution and high repeatability, and is thus suitable for large scale manufacturing. In the poster, we will also show case some emerging applications enabled by this technique.

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