The La Quinta Resort

La Quinta, California

November 3 – 7, 2019

Welcome to the 26th Lithography Workshop! With the support of its members, the Lithography Workshop has sponsored a unique program which is carefully designed to cover the latest lithography- related advancements to benefit all participants in their field of expertise. The Workshop held its first meeting in Lake Placid, New York in 1981. The 2019 Workshop is the 26th in a series of meetings that span 38 years, promoting the continuing evolution of lithography. The speakers at the Workshop are selected by invitation and represent a broad range of disciplines and covering a wide array of different lithography approaches and requirements. The Workshop is limited to 150 participants.

The Workshop is modeled to be similar to a "Gordon-Research" meeting but with the intent of addressing more immediate issues facing the lithography community within the next few years. The attendees of the Workshop share recent advances and knowledge in lithography with others in the community. The Workshop provides an environment where leading researchers from various disciplines can share their thoughts and ideas. A primary intent is to provide an arena for stimulating debate and the meeting schedule is designed to provide the attendees time for side-meetings and discussions. The Workshop has historically focused on leading-edge semiconductor applications but has also addressed the challenging lithography needs of flat panel displays, memory devices, 3- dimensional device integration and advanced packaging. Lately, the Workshop has showcased prominent experts in emerging fields like Quantum Computing and Artificial Intelligence, which are relevant to this audience due to the ubiquitous role lithography plays in the world of computing.

This is an opportunity for attendees to meet with world-renown investigators and discuss topics of mutual interest. The Workshop format is intended to provide an atmosphere for in-depth discussions of the invited presentations, both oral talks and poster papers. This is accomplished by providing time for extensive questions and answers after each paper, during the poster programs and during group meetings. This year, we will continue with opportunities to present, late-breaking topics of interest. As in the past, there will be no formal proceedings, picture taking, audio or video recording of the Workshop presentations. The technical sessions have been scheduled for mornings and evenings, with time for meetings between attendees and authors during the afternoon. Both invited and late breaking contributing Poster papers will be presented during the evening receptions, prior to the evening oral papers. Please see the Meeting's schedule of events for more information.

The Workshop welcomes student attendees! To encourage this, Student registration has traditionally been discounted; in recent years we have made available additional discounts to a few students in the form of lower rate hotel rooms. The Lithography Workshop is a non-profit organization, and the Committee believes that encouraging student participation is one of the best ways to return any small financial surpluses back to our community. The Executive Committee is arranging a program that we believe you will find intellectually stimulating and challenging. Putting together a meeting such as this required the contributions of many people. We are especially thankful to the Technical Program Chairpersons and the Session Chairs who have put together the program. This year, the Technical Program Chairs are Dr. Anton Devilliers (TEL) and Dr. Leo Pang (D2S). Each presentation (oral or poster) is invited, and each presenter is recognized for his/her outstanding work in their field.

We hope that you will avail yourself to all the sessions and functions that the organizers have planned. The Executive Committee welcomes your comments and suggestions to better serve the lithography community. The Lithography Workshop is very grateful to its sponsors, without whom, we would not be able to continue running the meeting. The LOGOs of our sponsors are shown on the back cover.

Vivek Singh
Intel Fellow, President of the Executive Committee

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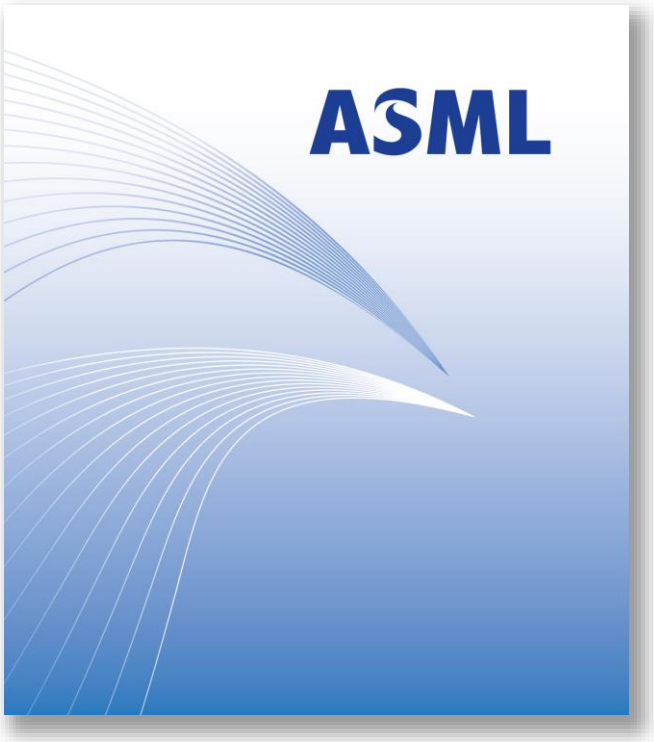

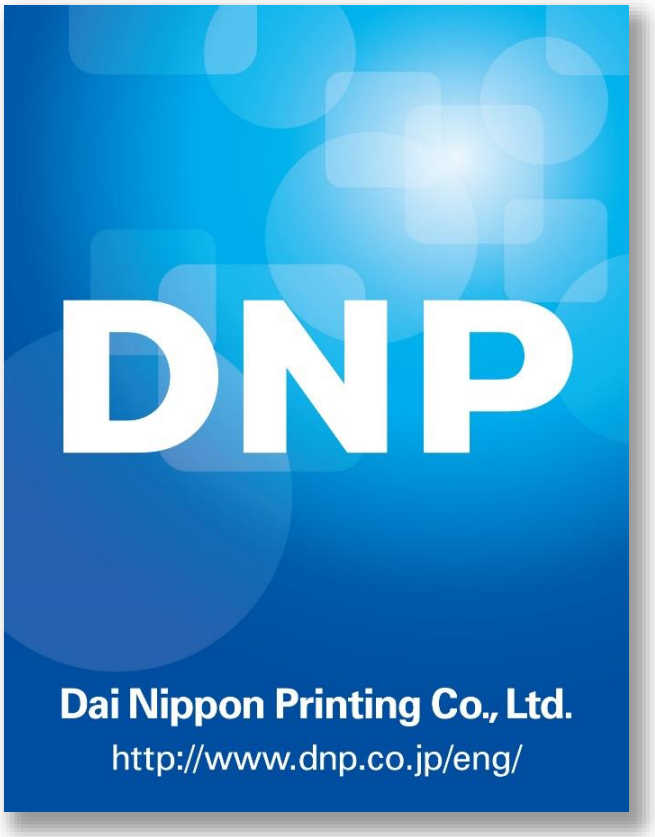

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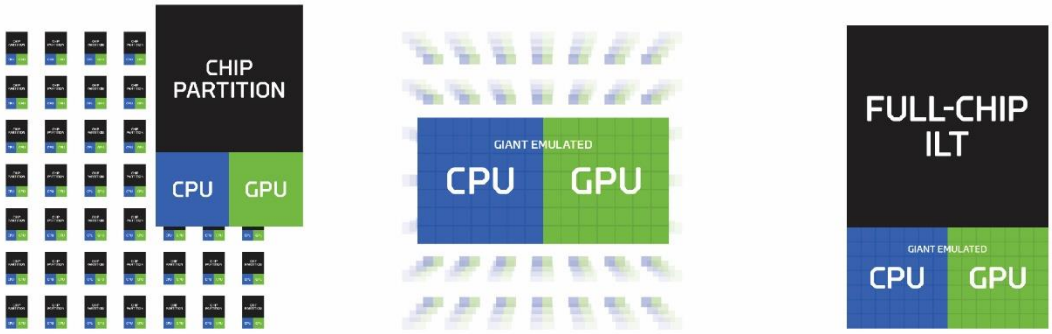

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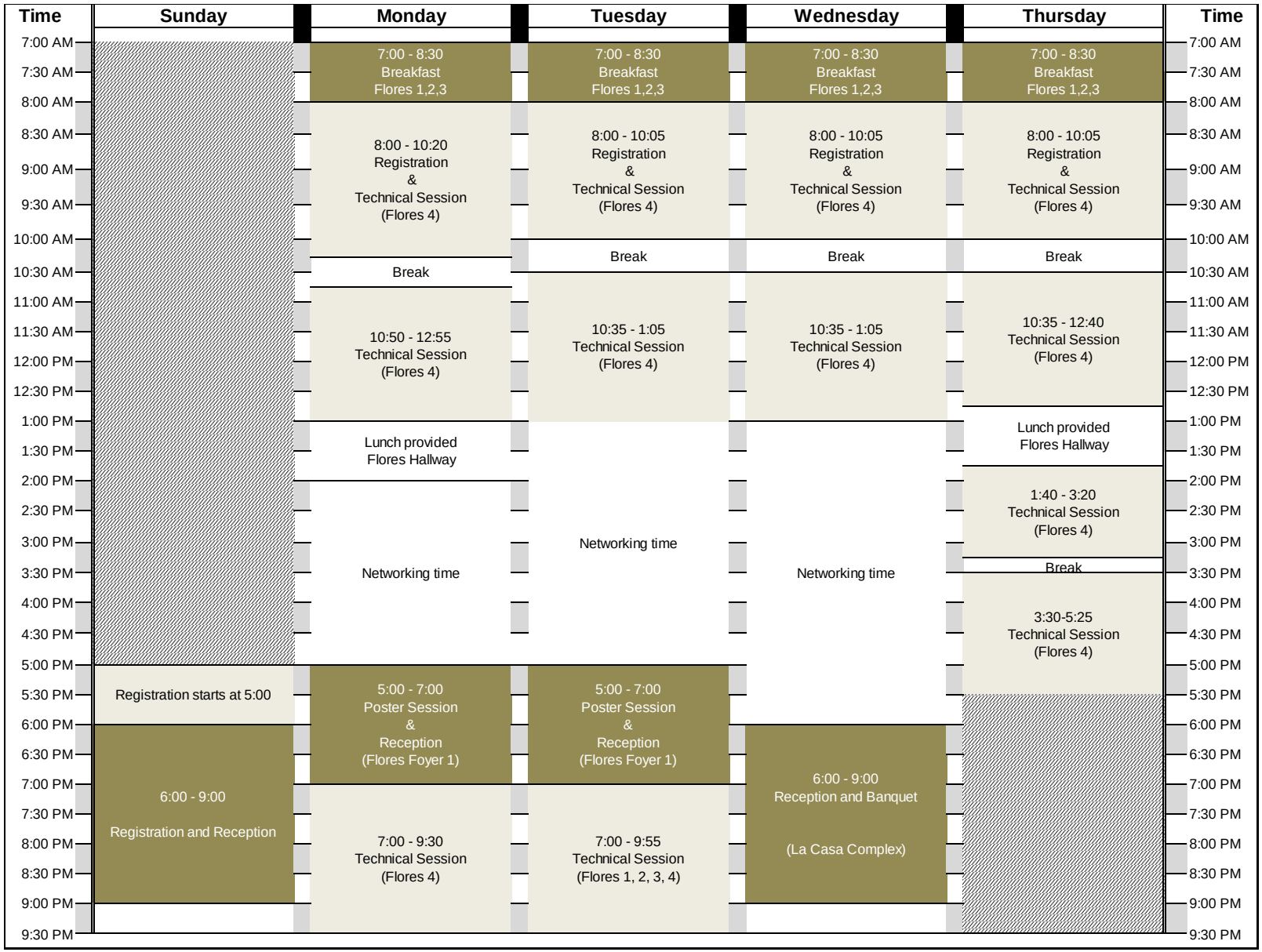
Advanced Materials and Process for Litho	Pat Martin (AMAT) Jeff Smith (TEL)
Multi Patterning Strategies	Bernd Geh (Zeiss) Donis Flagello (Nikon) Kamal Yadav
Metrology and Inspection	Thomas Scheurebl (Zeiss) Sterling Watson (KT)
E-Beam and Mask-Making	Noriaki Nakayamada (NuFlare) Bryan Kasprowicz (Photronics)
Computational Litho	Danping Peng (tsmc) Martin Burkhardt (IBM)
Topics in Advanced Packaging and 3D Design	Ravi Mahajan (Intel) Lars Liebmann (TEL)
AI & Deep Learning in Litho	Mike Meyer (CDLe) Yu Cao (ASML Brion)

SCHEDULE OF EVENTS



Schedule of Presentations

Monday, November 4, 2019

	Session Chairs: Britt Turkot, Leo Pang		
Session 1	8:00 – 8:15 AM	Vivek Singh	Welcome and Opening Remarks
	8:15 - 9:05 AM	Jos Benschop	***Plenary talk*: Lithography: the future is (not) what it used to be**
	9:05 – 9: 30 AM	John Petersen	Introduction to imec's AttoLab for ultrafast kinetics of EUV exposure processes and ultra-small pitch lithography
	9:30 – 9:55 AM	Naoya Hayashi	Multi-beam Technology for Advanced Mask Patterning
	9:55 - 10:20 AM	P. Jeffery Ungar	Stitchless Full Chip Curvilinear ILT in a Day
	10:20 – 10:50 AM	BREAK	

	Session Chairs: Yu Cao, Luigi Capodieci		
Session 2	10:50 – 11:15 AM	John Hu	An Intelligent Photon for the IC Industry - GPU AI Hardware for Deep Learning Applications
	11:15 – 11:40 AM	Stacey Bent	Area Selective Atomic Layer Deposition for Advanced Patterning
	11:40 AM – 12:05 PM	Kenji Yamazoe	Aberration impact on partially coherent imaging
	12:05 – 12:30 PM	Noriaki Nakayamada	Proposal of a new data format for multibeam mask writer with curve expression
	12:30 - 12:55 PM	Paul Schroeder	Multi-layer weak point detection and repair flow
	12:55 PM	End Session	

	Session Chairs: Da Yang, Donis Flagello		
Session 3	7:00 – 7:25 PM	Hiroki Miyai	Actinic Patterned Mask Defect Inspection for EUV Lithography
	7:25 – 7:50 PM	Marie Krysak	EUV Resists: Assessing High-NA Stochastics with Today's Tools
	7:50 – 8:15 PM	Yuri Granik	OPC for multi-patterning
	8:15 – 8:40 PM	Shashank Ekbote	Title to be announced
	8:40 – 9:05 PM	Prof. Peter Yuan	Artificial Intelligence Enhanced Place-and-Route of 3D Process-in-Memory Accelerators
	9:05 – 9:30 PM	Thomas Pistor	Applications of Pattern Matching in Lithography
	9:30 PM	End Session	

Schedule of Presentations

Tuesday, November 5, 2019

	Session Chairs: Noriaki Nakayamada, Mike Rieger		
Session 4	8:00 – 8:50 AM	Winfried Kaiser	***Plenary talk: The Evolution of Lithography Optics: From UV to EUV and beyond***
	8:50 – 9:15 AM	Siva Kanakasabapathy	Title to be announced
	9:15 - 9:40 AM	Andy Neureuther	EUV Lithography Fundamentals: Measurements and Models
	9:40 - 10:05 AM	BG Kim	New approach to EUV solutions for easy access to EUV HVM
	10:05 – 10:35 AM	BREAK	

	Session Chairs: Danping Peng, Ravi Mahajan		
Session 5	10:35 – 11:00 AM	Robert Bristol	High-NA stochastics: a method for making practical progress today
	11:00 – 11:25 AM	Linyong Pang	Making Digital Twins using the Deep Learning Kit (DLK)
	11:25 – 11:50 AM	Stephen Renwick	193nm lithography's path to the future
	11:50 AM – 12:15 PM	Andreas Olofsson	Title to be announced
	12:15 - 12:40 PM	Oliver Patterson	An In-Line Test Structure Approach for Quantifying Edge Placement Error
	12:40 - 1:05 PM	Andreas Erdmann	Perspectives & tradeoffs of novel absorbers for EUV lithography
	1:05 PM	End Session	

	Session Chairs: Mike Meyer, Martin Burkhardt		
Session 6	7:00 – 7:25 PM	David Fried	Technology Node Scaling Through Variation Control
	7:25 – 7:50 PM	James Shiely	Found in Translation
	7:50 – 8:15 PM	Stephen Hsu	EUV Imaging optimization to reduce the impact of wavefront aberrations
	8:15 – 8:40 PM	Vidya Vaenkatesan	Local Errors on EUV Mask and its Impact on Wafer
	8:40 – 9:05 PM	Ivan Ciofi	Calibrated Modeling of Line-to-Line Dielectric Reliability: LER Specs to Meet Reliability Constraints at Operating Conditions
	9:05 – 9:30 PM	David Chanemougame	Agile PPAC platform for fast exploratory DTCO: the LGAA CFET case
	9:30 - 9:55 PM	Nelson Felix	The Evolution of Patterning Challenges from High-Performance Computing to AI Applications
	9:55 PM	End Session	

Schedule of Presentations

Wednesday, November 6, 2019

	Session Chairs: Thomas Scherübl, Anton Devilliers		
Session 7	8:00 – 8:50 AM	Ravi Mahajan	***Plenary Talk: Advanced Packaging Architectures for Heterogeneous Integration***
	8:50 – 9:15 AM	Chris Progler	Is perfection the new standard for functionally matched photomasks ?
	9:15 – 9:40 AM	Ingo Schulmeyer	Corrected Low Voltage SEM for Metrology and Analytics
	9:40 - 10:05 AM	Michael Yeung	Use of GPU accelerated Maxwell solver in rigorous lithography simulation
	10:05 – 10:35 AM	BREAK	

	Session Chairs: Pat Martin, Jeff Smith		
Session 8	10:35 – 11:00 AM	Andrey Rudenkow	Unexpected Challenges in Material Quality at the Leading Edge
	11:00 – 11:25 AM	Samee Rehman	Optimizing Overlay using Machine Learning on Fab Context Data
	11:25 – 11:50 AM	Tetsuro Nakasugi	The future of NIL: enabling a new semiconductor manufacturing
	11:50 AM – 12:15 PM	Mike Green	Advanced modeling techniques for mask process development and verification
	12:15 – 12:40 PM	Brian Cline	DTCO in 2019: The Precious Metal Stack and the Route to Better Designs
	12:40 - 1:05 PM	Curtis Zwenger	Challenges Facing Photolithography in Advanced Packages
	1:05 PM	End Session	

Schedule of Presentations

Thursday, November 7, 2019

	Session Chairs: David Fried, Kafai Lai		
Session 9	8:00 – 8:50 AM	Scotten Jones	***Plenary Talk: Economics in the 3D Era***
	8:50 – 9:15 AM	Yuki Watanabe	Deep learning in lithography applications
	9:15 – 9:40 AM	Daan Slotboom	EUV-DUV matching in a world of 2nm overlay
	9:40 - 10:05 AM	Toshiyuki Hisamura	ACAP – Adaptive Compute Acceleration Platform and the Lithography Needs
	10:05 – 10:35 AM	BREAK	

	Session Chairs: Bryan Kasprowicz, Sterling Watson		
Session 10	10:35 – 11:00 AM	Chris Mack	Metrology for Roughness and Stochastic Variability Measurements and Why it is Essential for Making EUV Successful
	11:00 – 11:25 AM	Doug Resnick	Matching in a world of 2nm overlay
	11:25 – 11:50 AM	Martin Burkhardt	Investigation of mask absorber induced image shift in EUV lithography
	11:50 AM – 12:15 PM	Rahul Lakwawat	Optical Inspection for EUV ADI Defectivity
	12:15 - 12:40 PM	Peng Liu	Mask Synthesis using Machine Learning Software and Hardware Platforms
	12:40 PM	End Session - Lunch provided	

	Session Chairs: Bernd Geh, Martha Sanchez		
Session 11	1:40 – 2:05 PM	Clemens Utzny	Application of machine learning methods to lithographic problems
	2:05 – 2:30 PM	Joe Ervin	Assessment of Various Patterning Integration Options Using Virtual Fabrication
	2:30 – 2:55 PM	Peter Buck	Machine Learning Guided Curvilinear MPC
	2:55 - 3:20 PM	J. Alexander Liddle	Bottom-up fabrication: Promises and Pitfalls
	3:20 PM	End of session	

	Session Chairs: Lars Liebman, Kamal Yadav		
Session 12	3:30 – 3:55 PM	Jeffrey Smith	Here there be dragons – what lies at the end of the area scaling roadmap
	3:55 – 4:20 PM	Pieter Weckx	Scaling solutions in the 3rd dimension
	4:20 – 4:45 PM	Henry Kamberian	EUV Mask Technology: Challenges and Opportunities on Path to N3 Requirements
	4:45 - 5:10 PM	John Randall	The Next Generation of Ultra-High Resolution E-Beam Lithography
	5:10 – 5:25 PM	Closing Remarks	
	5:25 PM	End Session and Conference	

Poster Papers

Monday, November 4, 5:00 – 7:00 PM
Tuesday, November 5, 5:00 – 7:00 PM

Presenter	Title
Alex Tritchkov	Use of Native Objective Functions in Pixel-based Mask Optimization
Derren Dunn	Title to be announced
Farhang Yazdani	Wafer/Panel level Fan-out Enabling Heterogeneous Chiplet Integration
John Peterson	Update of EUV Resist Evaluations at imec
Juhao Wu	Enhancement Cavity and Coating for Accelerator-Based EUV Sources for Lithography
Luigi Capodieci	Search and ML Applications of Pattern Matching in Lithography and DFM
Neils Wijnaendts van Resandt	Technology challenges in industrial high-speed direct write lithography
Ofir Sharoni	Excursion Prevention Strategy to increase Chip Performance by Photomask Tuning
Regina Freed	Materials Engineering Solutions to Extend DRAM Scaling
Ric Borges	Title to be announced
Shimon Levi	Title to be announced
Takahiro Mori	aquaSAVE™: Antistatic Agent for Electron Beam Lithography
Vikram Tolani	Computational Techniques Enabling EUV Mask Defect Disposition
Yuhang Zhao	AI Computational Lithography

Session 1

Presentation Schedule for
Monday, November 4, 2019

Session Chairs
Britt Turkot
Leo Pang

	Time	Presenter	Title
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	10:20 – 10:50 AM	BREAK	

Lithography: the future is (not) what it used to be.

Jos Benschop
ASML

Lithography has been the key enabler for Moore's Law over many decades.

As pointed out by Gordon Moore in his 1995 SPIE presentation, the "contribution from increased density from finer line widths has been constant over the last 25 years", a trend which continues to this day.

For decades this has been made possible through a combination of wavelength reduction, increased numerical aperture (NA) and pushing imaging closer to the physical limit (low-k1).

Over the last decade double patterning and spacer technology enabled the industry to have pattern lines significantly below the resolution limit of single exposure which equals 38nm half pitch for a NA=1.35 ArF scanner.

With the introduction of NA=0.33 EUV into volume manufacturing the imaging capability of optical scanners is back on its historical trend. The realization of a NA=0.55 EUV scanner is well on its way and will ensure geometrical shrink continues well into the next decade.

As Gordon Moore pointed out in his 1975 paper, lithography is not the only driver. He showed that from 1965-1975 "die size" and "device an circuit cleverness" made a contribution similar to "dimensional reduction". Today Moore's Law is again firing on three cylinders: the traditional "dimension scaling" and "device and circuit cleverness" complemented by going into the third dimension.

In the presentation we will show how a holistic view on lithography (including scanner, metrology and computational power) has enabled a cost effective shrink over the last decades, and how it will continue to do so for the foreseeable future. The introduction of EUV brings unprecedented imaging capability and some new challenges like increased stochastically variations. Challenges and potential solutions will be shared. Finally the litho challenges and solutions going into the 3rd dimension will be shared.

Introduction to imec's AttoLab for ultrafast kinetics of EUV exposure processes and ultra-small pitch lithography

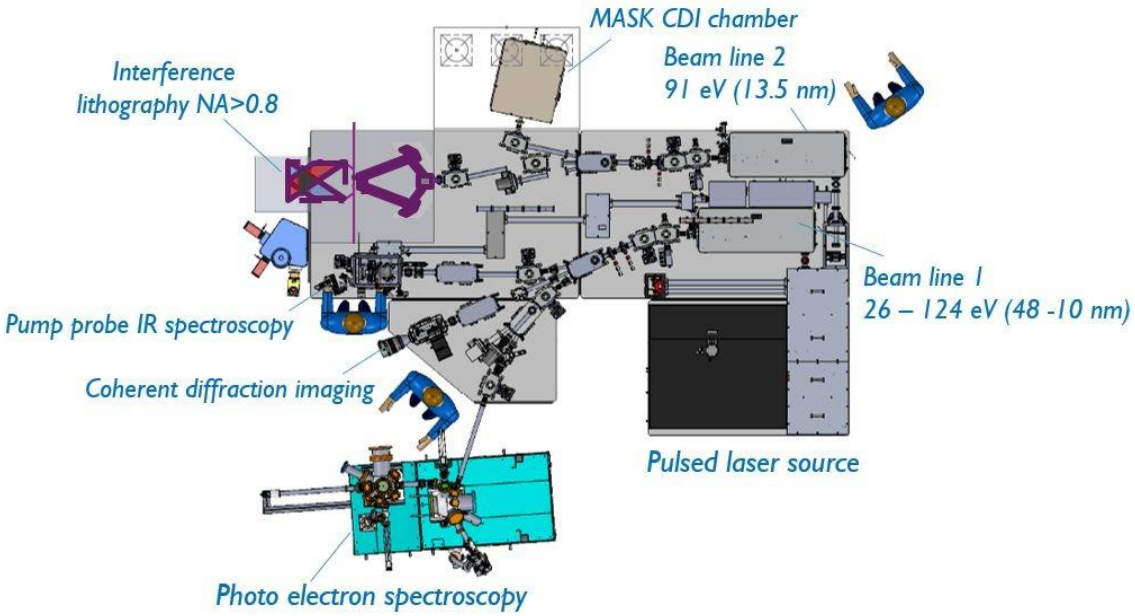
John Petersen and Paul van der Heide
Imec, Leuven BE

Recently, imec announced, with joint development partners, KMLabs and Spec's, plans to build the first industrial laboratory capable to monitor the 13.5 nm, EUV exposure process from initial photon absorption, in the attosecond range, and, progressively tracking, to 200 picoseconds the subsequent photoionization, and its resultant cascade of secondary electrons and chemical process that occur. This ability will enable for the first time understanding of high energy processes that influence final resist chemistry that will in turn be used to develop better resists for high numerical aperture imaging and lithography modelling for process and OPC design.

To accomplish this, the lab uses time-resolved: Infrared spectroscopy, photoemission electron microscopy spectroscopy (PEEMS) ultraviolet photoelectron spectroscopy (UPS), and x-ray photo electron spectroscopy, XPS to construct a picture of the molecular dynamics of the EUV exposure process with the aid of density field theory molecular and molecular dynamic simulation. In addition, beyond resists, using angle-resolved photoemission spectroscopy (ARPES) other time resolved material phenomena can be explored and understood, such as topological insulators, semi-metals and other beyond Moore's law and quantum computing device materials.

In addition, using the coherence of its high harmonic generated sources from KMLabs, the AttoLab will do interference lithography from 32 nm to 8 nm pitch, as well as lensless imaging using electron reflectometry. The lithography will allow the probing of resist chemistries near their molecular limits. The lensless imaging will be looked at for inspection and SEM and AFM supplemental imaging techniques that has the added capability of examining subsurface topography.

The presentation will review the laboratory and will survey the science and technology that it enables.



Multi-beam Technology for Advanced Mask Patterning

Naoya Hayashi
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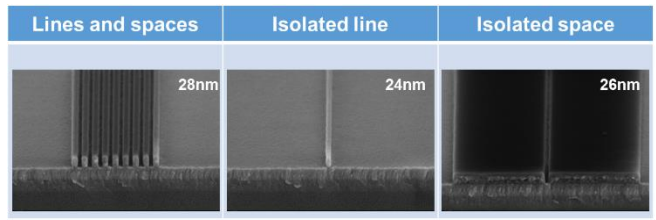
Multi-beam mask writer has been essential for patterning the complex and precise features on advanced masks with reasonable writing time. MBMW-101 from IMS Nanofabrication GmbH has been used worldwide, equipped with 262-thousand programmable beams, and an air-bearing stage by JEOL.

The tool performances with 20nm beams were evaluated for photomask application. The result showed remarkable performances. The resolution on photomask has reached less than 30nm with negative CAR (Chemical Amplified Resist) (Fig.1.). The global position accuracy is around 1nm in 3sigma across the mask. The any angled pattern resolution was also evaluated, and 100nm gap angled patterns were smoothly resolved (Fig.2.). The tool performances with 10nm beam were also evaluated for NIL (Nanoimprint Lithography) template requirement. By using specific low sensitivity resist, less than 15nm lines and spaces were resolved across the full field, 26 mm x 33mm, of the template (Fig.3.).



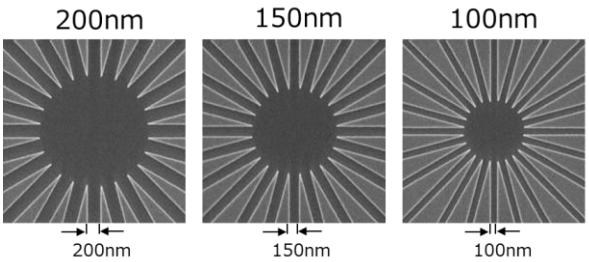
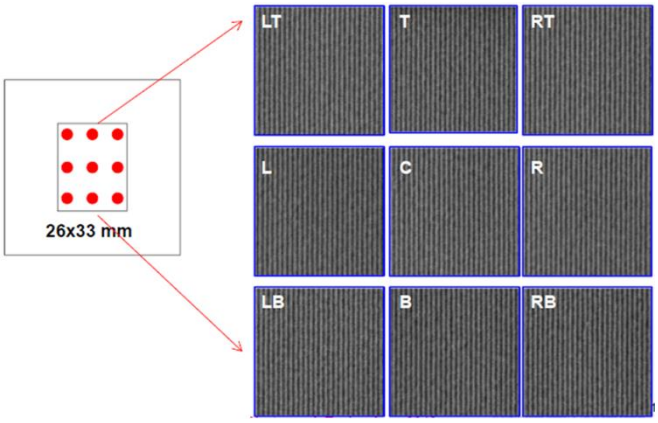


Fig.1. Pattern resolution of MBMW with negative CAR.

Fig.2. Pattern fidelity of any angle patterns.

Fig.3. Full field 14nm lines & spaces resolution on nanoimprint template.



Stitchless Full Chip Curvilinear ILT in a Day

P. Jeffrey Ungar
D2S, Inc.

It is has been generally accepted that Inverse Lithography Technology (ILT) methods applied to full-scale layouts are much too slow to compute, suffer from inevitable stitching problems at tile boundaries, and produce masks that take too long to process and write. Multi-beam mask writers can address the last objection through constant write times independent of mask complexity, but the speed and stitching issues have relegated ILT to hot-spot fixing and solving small areas like periodic structures. In this presentation, I describe how we have achieved stitchless, full-chip ILT in a day through a combination of mathematics and physics, high performance computing (HPC) methods, GPU acceleration, and tailoring our computational design platform (CDP) to the task.

We began by formulating ILT in a mathematically consistent way to enable high quality results. This led us to use a pixel-style representation, which also enabled a single-instruction, multiple-data (SIMD) model of GPU acceleration. (We do not use geometric representations at any time during ILT solution. We produce final mask geometry through a simple post processing step.) Stitching problems arise in conventional ILT from dividing up the layout into manageable tiles and solving these separately. This obtains easy parallel execution, but the solutions are often inconsistent across tile boundaries even when allowing for a substantial ambit. Instead of solving independent tiles, we solve the whole chip together using HPC techniques.

Solving for the entire layout together efficiently requires a CDP that is tailored to stitchless ILT, not only to provide sufficient computational resources (GPUs and CPUs) and an interconnect that supports fast exchange of data, but also enough RAM to hold all the data that is “in-flight” while ILT optimization proceeds. The combined system exhibits excellent strong scaling.

Session 2

Presentation Schedule for
Monday, November 4, 2019

Session Chairs
Yu Cao
Luigi Capodieci

	Time	Presenter	Title
Session 2	10:50 – 11:15 AM	John Hu	An Intelligent Photon for the IC Industry - GPU AI Hardware for Deep Learning Applications
	11:15 – 11:40 AM	Stacey Bent	Area Selective Atomic Layer Deposition for Advanced Patterning
	11:40 AM – 12:05 PM	Kenji Yamazoe	Aberration impact on partially coherent imaging
	12:05 – 12:30 PM	Noriaki Nakayamada	Proposal of a new data format for multibeam mask writer with curve expression
	12:30 - 12:55 PM	Paul Schroeder	Multi-layer weak point detection and repair flow
	12:55 PM	End Session	

An Intelligent Photon for the IC Industry
- GPU AI Hardware for Deep Learning Applications

John Hu
Nvidia Corporation

The massively parallel processing nature of GPU and AI DLA architectures has enabled scaling up of computing power to handle the massive data and large DNN models. Today's state of the art AI chip in the market, GV100, has 277 billion transistors in a 2.5D Interposer integrating Volta GPU/DLA & HBM2. To enable good yield and reliability of this reticle size chip, defect per trillion level is required. Furthermore, with the automotive reliability requirements, the industry is driving towards zero defect.

As the device dimension shrinks, a "normal" variation or distortion in nm range from litho or etch, can kill yield or reliability. These challenges have slowed down Moore's Law in past few years. On the other hand, the rapid improvements in architectures and algorithms have driven AI computing performance to improve ~100x in past few years. As we are entering the era of architecture driven growth, the IC technology, particularly litho, needs to improve further to overcome the scaling challenges, to become part of the factor in enabling 1000x compute efficiency required by AI computing in next decade.

The progress in GPU and AI compute has also provided additional tools to solve the problem in designing and productizing future giga chips. AI applications have been used extensively in IC design, OPC and mask making, IC processing, tools matching and control, quality & productivity improvements, inline parametric check & defect inspection, yield & functionality analysis etc. CNN and GAN are also used to ensure the patterns processed on wafer matches closely to design intentions.

AI algorithms and applications have also grown exponential in the past few years. Machine learning, especially GAN etc., has also enabled re-construction of ground truth from partial information, as well as other exciting applications that will be discussed in more details. Ray tracing capabilities are built in GPU chips since Turing generation, rendering photons with realistic lighting effects in the compute intensive physics simulations.

In the coming new technology nodes, only a small quantity of photons is present to print a pattern on the wafer, or in inspecting a feature for defects. The random variation of these photons can become dominating factor. It will be more critical for a more intelligent way in processing and in defect detection. This will require each photon to be intelligent, aided by GPU AI computing.

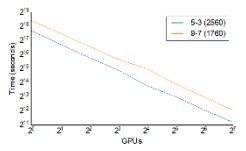


Fig1. GPU performance scales with GPU counts (ref: Baidu, Deep Speech 2: End-to-End Speech Recognition in English and Mandarin, 2015)

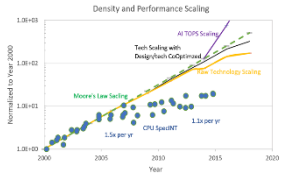
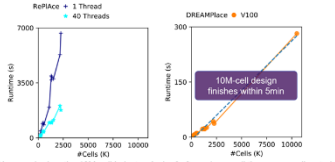


Fig2. The Era of Architecture Driven Performance Improvements after the Slow Down of Moore's Law



RePlAce crashed on the 10M-cell industry *design6* after using up all the memory allocated

Fig. 3. DL and GPU to accelerate VLSI design (Yabo Li et al, GTC2019)

Fig. 4a. Image Impainting for irregular Holes using GAN (Guilin Liu et al, ECCV 2018);

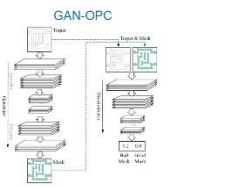


Fig 4b. Gan OPC (H. Yang et al, DAC 2018)

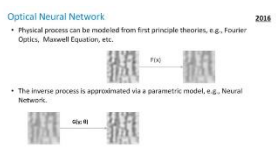


Fig 5. Physics Based AI for Semiconductor Inspection Using a GPU Based Optical Neural network (J. Zhang et al, GTC2018)

Area Selective Atomic Layer Deposition for Advanced Patterning

Stacey F. Bent
Department of Chemical Engineering, Stanford University, Stanford, CA, 94305 USA

The rapid growth of technologies such as machine learning and autonomous vehicles is fueling a need for more powerful electronic chips, and the semiconductor industry is working to meet this need with ever-more complex nanoscale device structures. With the growing demands on nanostructure fabrication, selective deposition is gaining attention as an important process to achieve pattern features at the sub-10 nm length scale. Selective deposition is a bottom-up growth strategy in which material is added only where desired, without the need for subsequent lithography and etch steps. Both two-dimensional planar geometries and three-dimensional structures will benefit from selective deposition processes, with advantages in reduced process complexity and improved pattern fidelity.

In this presentation, we will describe how control over the substrate surface properties using molecular monolayers can achieve area selective atomic layer deposition (ALD). ALD relies on self-saturating, layer-by-layer, gas-surface reactions to deposit conformal thin film materials. ALD is a good choice for selective deposition because its chemical specificity provides a means to achieve selectivity on a spatially patterned substrate. In particular, inhibitory layers such as self-assembled monolayers (SAMs) can alter the native surface reactivity, allowing ALD selectivity to be achieved. We will show that this process provides good selectivity for thin deposited films, and demonstrate selective deposition on different materials, including dielectrics and metals such as Cu, Co, W and Ru. Strategies to achieve even higher selectivity will be described, including repairing the inhibitory layer between ALD cycles and adding a selective etching step. We will also overview challenges that need to be overcome in order to achieve atomic-scale precision on nanoscale patterns, particularly at interfaces. Directions toward new area selective deposition processes will be presented.

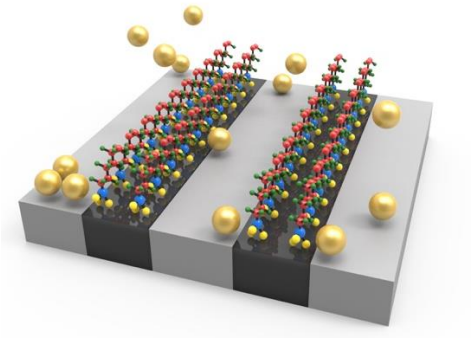
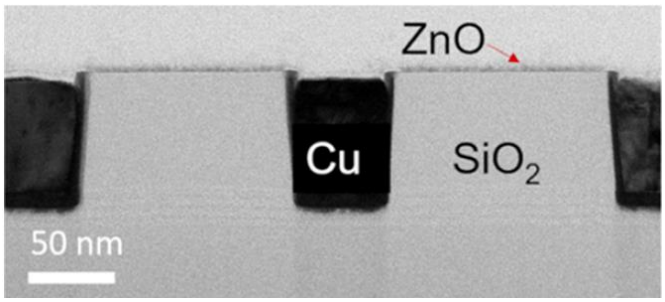


Illustration of an area selective ALD process using inhibitor molecules



TEM image of ~2 nm-thick ZnO film deposited selectively on SiO_2 regions of a Cu/dielectric pattern

Aberration impact on partially coherent imaging

Kenji Yamazoe and Danping Peng
TSMC Technology Incorporated, 2851 Junction avenue San Jose, CA 95134

Advanced lens design technique, continuous fabrication improvement of lens, robust and dedicated mechanical structure of the lens barrel, and careful wavefront measurement significantly reduced the wavefront aberration of optical lithography. Currently, in ArF (193nm exposure wavelength) lithography, the aberration is negligible.

EUV (13.5nm exposure wavelength) lithography is, however, challenging from the view point of aberration. Mirrors are used in EUV optics. As its reflectivity is approximately 70%, the EUV optics can use only 6 or 8 mirrors to have enough exposure dose on wafer, which induces complicated lens design with strong aspheric mirrors difficult to fabricate. Yet, let us assume we can achieve the same fabrication error in ArF and EUV and see how the aberration is. For example, if there is a 1nm fabrication error on a portion of the lens surface of ArF lithography, wavefront error at that portion would be reduced approximately to half (0.5nm) thank to the refractive optics with lens refractive index of approximately 1.5. However, 1nm fabrication error of the EUV mirror would be doubled to approximately 2nm wavefront error due to the reflection. Furthermore, the impact of wavefront aberration on imaging is determined by its relative value to the exposure wavelength. If the aberration has 1nm RMS (root-mean-square), it is 0.005λ RMS for ArF lithography whereas it is 0.074λ RMS for EUV lithography. Therefore, EUV mirror fabrication requires much tighter error control compared with ArF lens. We cannot forget about wavefront measurement. Because we have limited optical elements for EUV light, establishment of precise wavefront measurement system for EUV optics is also challenging. For these reasons, we aware of aberration of EUV optics more than that of ArF optics.

Aberration impact of imaging is a continuous interest for optical engineers and we can find many literatures which address it. However, now that EUV lithography is ready, it is a good timing to review the aberration in optical system. In the talk, we will first talk about the general concept of wavefront aberration. Next, a brief note for the simulation with aberrated optics is presented. Lastly and mostly, we focus on how the aberration impacts imaging under partially coherent illumination.

Proposal of a new data format for multibeam mask writer with curve expression

Noriaki Nakayamada[a], Kenichi Yasui[a], Thiago Figueiro[b], Matthieu Millequant[b], Patrick Schiavone[b]
[a] NuFlare Technology, Inc. [b] Aselta Nanographics

We propose a new data format using curve expression for the multibeam mask writer. We would like to discuss its necessity, format candidate, prospected user, and timing of introduction in the conference.

1. Why new format is necessary

The fundamental limit of a single-beam variable-shaped mask writer is that it can write only a few types of shapes by a single shot. Multibeam mask writer has removed this restriction by converting any shapes into a bitmap of fixed-size pixels so that multiple pixels can be exposed simultaneously. Then the best data format for multibeam mask writer shall be a bitmap instead of polygons however the time is not mature yet to adopt bitmap data format in every front of photomask or wafer manufacturing, not to mention about the difficulty of getting agreement on the unified pixel size among all the stakeholders. During this transition period from polygons to bitmap, we propose alternative way of expression of curvilinear pattern using curve formula.

2. How curvilinear patterns are expressed

We propose spline-based expression in defining the boundary of a curvilinear pattern. We also tested several different formulae and their comparison will be presented in the conference. We found that ordinary Manhattan shapes are hard to be expressed by curve formula, so we propose a hybrid of conventional polygon definition and new curve definition in the new format. We will discuss pros and cons between simple loss-less compression of bitmap versus lossy geometric compression by curves.

3. Who will get benefits from the new format

Any EDA, writer, inspection tool vendors in photomask and wafer manufacturing should get the benefit from the new format through its data compaction, as long as lossy compression is acceptable. In other words, acceptable edge placement error (EPE) will decide whether the new format is beneficial or useless. Once it is adopted, all sectors should adopt it because one sector converting curves to polygons in the middle of the manufacturing flow will eliminate the benefits for curves in the later steps.

4. When the new format will be needed

We anticipate that the new format will be necessary when EUV starts using ILT, unless unified bitmap format and good compression/decompression algorithm are publicly formalized until then.

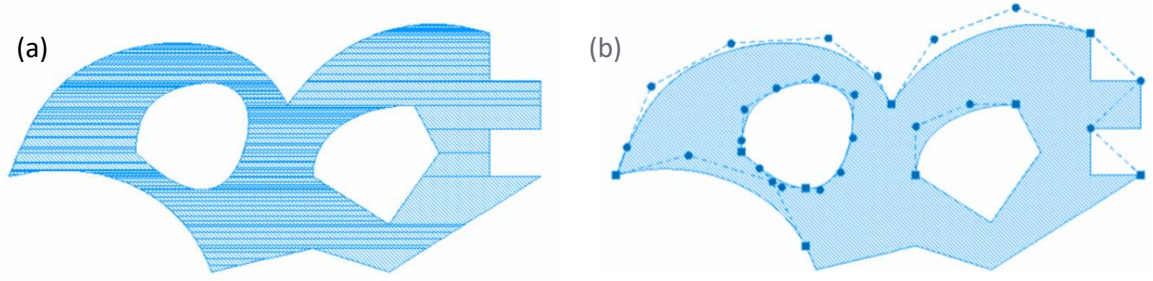


Figure.1
Example of curvilinear pattern defined by (a) conventional polygons and (b) proposed curve format

Multi-layer weak point detection and repair flow

Uwe Paul Schroeder, Janam Bakshi, Ahmed Mounir Elsemary, Omnia Mohamed,
Fadi Batarseh, Pouya Rezaeifakhr, Shobhit Malik, Sriram Madhavan
GLOBALFOUNDRIES, 2600 Great America Way, Santa Clara, CA

One of the challenges of advanced node multi-patterning technologies is to de-convolute the complex layer to layer interactions into universally applicable fail point detection definitions. Specifically very hard to meet is the requirement that such a detection method can be run on large designs within a reasonable time. ORC has progressed over the years such that undetected printability fails within one layer are now relatively rare, but pinpointing multi-layer patterning issues in ORC is still a problem, especially in complex 2D design situations.

Meanwhile, full design pattern profiling has become a mainstay of the industry, and can add a lot of value by cataloguing possible configurations. Our paper demonstrates a flow for finding multi-layer weak points. We start from describing known fail modes first, and then making the connection to the corresponding pattern space. Based on a well-known via open fail mechanism, where the projected Self-Aligned Via (SAV) area of the top metal is getting too small in process window corner conditions, we define a multi-layer printability check using derived multi- layer contours.

A representative set of sample clips is harvested from full design pattern profiling and gets fully analyzed for this failure mode. The distribution of the minimal projected SAV area in OL and CD process corners gets recorded. Out of that distribution, the tail end at the small side of the SAV area is used for further pattern refinement. If proven to have systematic yield weakness, the patterns are then added to a bad pattern database. That database is provided to foundry customers and called in the router techfile during place & route, where the bad patterns are detected and can either be fixed or avoided. This can reduce the occurrence of the potential process window limiters significantly in new designs, without sacrificing area or performance.

Session 3

Presentation Schedule for
Monday, November 4, 2019

Session Chairs
Da Yang
Donis Flagello

	Time	Presenter	Title
Session 3	7:00 – 7:25 PM	Hiroki Miyai	Actinic Patterned Mask Defect Inspection for EUV Lithography
	7:25 – 7:50 PM	Marie Krysak	EUV Resists: Assessing High-NA Stochastics with Today's Tools
	7:50 – 8:15 PM	Yuri Granik	OPC for multi-patterning
	8:15 – 8:40 PM	Shashank Ekbote	Title to be announced
	8:40 – 9:05 PM	Prof. Peter Yuan	Artificial Intelligence Enhanced Place-and-Route of 3D Process-in-Memory Accelerators
	9:05 – 9:30 PM	Thomas Pistor	Applications of Pattern Matching in Lithography
	9:30 PM	End Session	

Actinic Patterned Mask Defect Inspection for EUV Lithography

Hiroki Miyai, Tsunehito Koyama, Hal Kusunose
Lasertec Corporation

As EUV lithography enters high volume manufacturing, the semiconductor industry considers actinic patterned mask inspection (APMI) to be the major remaining EUV infrastructure gap. The IC industry has called for APMI for over 20 years. Until APMI tools are deployed, the IC industry is bridging the gap by stretching existing mask inspection tools and wafer inspection processes.

There are multiple issues with these APMI work-arounds. Wafer printing test is challenging. In addition, high-sensitivity wafer inspection becomes extremely difficult because a 10% delta-CD defect is hard to find and classify in the presence of the stochastic patterning noise inherent in EUV lithography. DUV mask defect inspection tools require four to six inspection passes at different optical configurations to achieve moderate defect sensitivity on EUV masks. Even with these multi-pass inspections, DUV tools fail to find all of the desired EUV mask defects. Inspecting a 13.5nm EUV mask with 193nm DUV is analogous to inspecting an 193nm mask with a mid-infrared wavelength of 2760nm. DUV patterned mask systems do not claim to detect the phase defects in the EUV multi-layer that can cause 10% delta CD wafer print errors.

Combining experiences gained from developing and commercializing the 13.5nm EUV actinic blank inspection system (ABI) with 43 years of patterned mask defect inspection system manufacturing, we have developed the world's first high-sensitivity, high-speed actinic patterned mask inspection & review system. Major sub-systems were improved or added to transform the dark-field ABI system into the bright-field APMI system. Higher-intensity EUV source, higher-NA EUV optics, and higher-speed image processing systems enable actinic patterned mask inspection. We will report on the patterned mask defect detection sensitivities that are being demonstrated. We will conclude that APMI enables reliable detection of all classes of EUV-printable mask defects: small absorber defects, phase and amplitude defects in the multi-layer, and EUV-wavelength-specific flaws. Actinic inspection ensures that the mask going to the scanner is free from printable defects that may have been overlooked during EUV blank manufacturing or occurred during EUV mask manufacturing, cleaning and use.

EUV Resists: Assessing High-NA Stochastics with Today's Tools

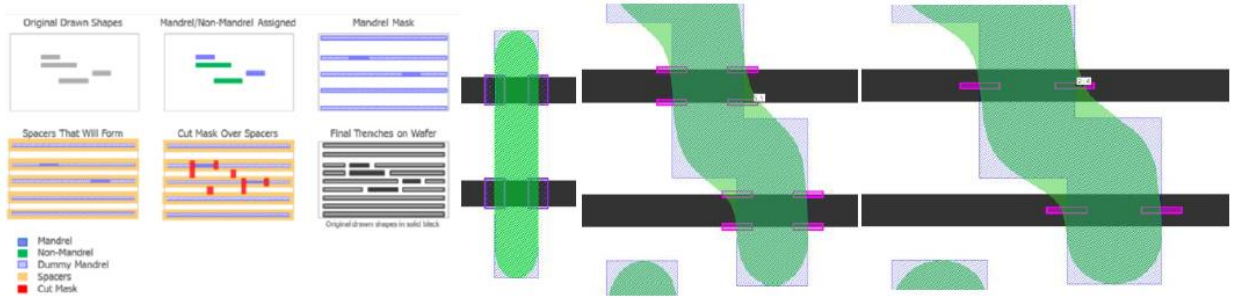
Marie Krysak, Iulian Hetel, Robert Bristol
Intel Corporation

Stochastic variations will be the leading yield limiter as we scale to feature sizes below 20nm. Sizeable efforts to improve photon stochastics and resolution are underway, including the development of High-NA tools and improving source power to deliver more photons. As a result, material stochastics are emerging as the limiting factor. We developed a method to assess stochastic risk of current resist platforms, without the need to measure large numbers of features. We evaluated several best-in-class resist platforms, including CARs, non-CAR polymers, and molecular resists, and show a clear stochastic advantage of novel resists at relaxed pitch over best-in-class CARs. This paper discusses the correlation of the patterning mechanism and stochastic failure risk, and highlights paths forward to designing high contrast, low noise resists.

OPC for multi-patterning

Yuri Granik
Mentor, a Siemens Business

Multi-patterning (MP) pioneers Greschner and Trumpp from IBM in 80th, Water Lur and C-H. Huang, both form UMC, and Micron engineers C. Roberts in 90th, then G. Sandhu in 2000th, have to be credited for the invention of various double-pattering tricks. The alternating phase-shifting (AltPSM) with two masks was considered - as an option - for 65 nm process by Intel [1]. Later Intel used second mask for the line-cutting at 45nm node, and TSMC at 28nm node. Later double patterning became ubiquitous at 20 nm node. Within the optical proximity correction (OPC) domain, Mentor Calibre® engineers became aware of mathematical and geometrical intricacies of layout decomposition into two "colors" while implementing AltPSM decomposition [2] in the end of 90th. Now the leading edge 5 nm and 3 nm technological nodes are made lithographically feasible - and profitable - by combining DUV multi-pattering with EUV. This ensue edge placement error (EPE) overlay and alignment challenges between non-homogenous scanners; these challenges have been enumerated in [3]. From the design and mask-making prospective, software-wise, we observe the following trend: MP complexities are being pushed up-stream of OPC, sometimes all the way to IC design stage, and almost always to the OPC pre-processing. With introduction of litho-friendly layout restrictions, a "zoo" of multi-pattering techniques have been culled to the self-aligned double patterning (SADP), self-aligned litho-etch (SALE), litho/etch double- (LELE), triple (LE_3), and quadruple- pattering (LE_4). Irregular non-gridded designs, color-conflicted layouts, and complex blocking masks are outlawed. Currently a typical foundry applies either SALE with 4 masks or LE_4 to Metal 0 layer, SALE with 3 masks or LE_3 to Metal 1 layer, a no-cut mask SALE for M2, LELE to contacts and vias, and LELE, or even LE_3 for the rest of the metal layers. Mentor Calibre® suite supports all these options, from the time of manual layer drawing, interactive and batch physical verification, automated multi-pattern decomposition, to the post-signup foundry-run verification of MP-induced design rules, pre-OPC retargeting, and to the final MP mask corrections and fracturing.



SADP and location of OPC sites for edge placement errors in SADP and SALELE processes, from [4, 5].

1. Yan A. Borodovsky, et al., "Lithography strategy for 65-nm node", Photomask Japan, 2002.

2. C. Spence, M. Plat, E. Sahouria, N. Cobb, F. Schellenberg, "Integration of optical proximity correction strategies in strong phase shifters design for poly-gate layers", Photomask Technology, 1999.

3. M. Phillips, https://nikonereview.com/2017/intel-and-nikon-technologists-assess-status-and-future-of-lithography

4. Y. Drissi, et al., "SALELE Process from Theory to Fabrication", joint IMEC/Mentor paper, Design-Process-Technology Co-optimization for Manufacturability, 109620V, SPIE 2019.

5. D. Abercrombe, et al., "Fill/cut SADP with Calibre® multi-patterning", Mentor's white paper.

Title to be announced
Shashank Ekbote
Qualcomm

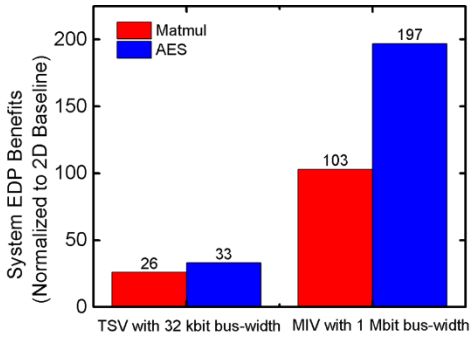
Artificial Intelligence Enhanced Place-and-Route of 3D Process-in-Memory Accelerators

J. Lin[1], M. Salem[1], J.-S. Yuan[1], L. Liebmann[2], J. Fulford[2], and A. Devillers[2]
[1]Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816
[2]TEL Technology Center, American, Albany, NY 12203

In recent years, Moore's law is slowing down. The gap between successive generations of chips with new, smaller transistors is widening, as it becomes increasingly more difficult to miniaturize transistors in a cost-effective way for production. In this work, we show an alternative way to technology scaling for machine learning and security related tasks, i.e., process-in-memory accelerators incorporating monolithic 3D (M3D) integration. With the M3D integration, CPUs and memories can be integrated into a single silicon, and Monolithic Inter-Tier Via (MIV) arrays are used to construct the data buses. Owing to the small pitch (in the range of 100 nm), the density of the MIVs is much higher than that of TSVs (its pitch size is around 5 µm) based on today's 3D integration technology. Thus, we obtain much higher bus widths and much lower parasitic capacitances with M3D. This could overcome the performance bottleneck resulting from intensive data movements. We model the architecture using GEM5 and adopt an eight-core CPU as the benchmark. Due to the high bandwidth of the memory buses of the M3D architecture, we remove the L2 and L3 caches to save energy consumption and reduce the delay for hierarchical accessing. We employ two applications to simulate our architecture. One is the matrix multiplication, which is the fundamental operation in machine learning algorithm. The other one is the Advanced Encryption Standard (AES), which is dominated by shift and XOR operations. The architecture configuration and simulation results are shown in Fig. 1. We also compare the simulation result from the same architecture using TSVs to show the benefit of pitch size reduction. From Fig. 1 the M3D architecture can obtain 5x EDP reduction to the architecture with TSVs and over 100x EDP reduction to the CPU benchmark.

	CPU (2D Baseline)	PIM (3D)
# of Cores	8	8 (could be much higher)
L1 Cache	64 kB	64 kB
L2 Cache	256 kB, private	NA
L3 Cache	2 MB, shared	NA
MEM bus width	64 bit	MIV: 1 Mbit TSV: 32 kbit (data from N3XT paper)
MEM bus frequency	800 MHz	800 MHz

(a)



(b)

Fig. 1 (a) Architecture configuration (b) normalized EDP compared to a CPU benchmark.

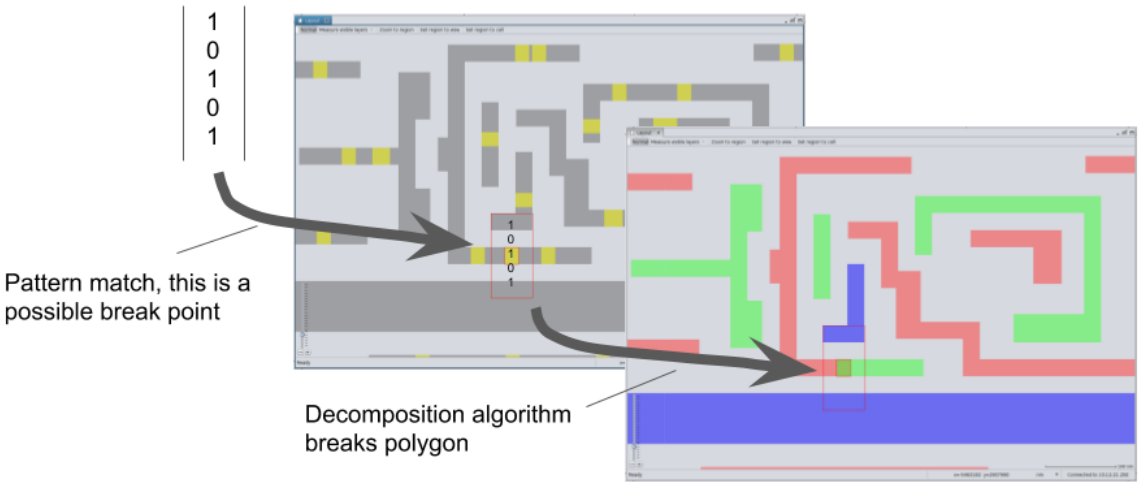
To physically implement our architecture, we synthesize the RTL design with Synopsys Design Compiler. The netlist is parsed into a graph and label propagation to partition the tiers. Moreover, an artificial intelligence based algorithm is employed to ensure the optimization of tier assignment considering wire-length, density, and number of MIVs. This 3D floor-planner consists of rough placement, optimization, tier assignment, and MIV insertion modules. Having partitioned the netlist into different tiers, the place and route are performed with Synopsys IC Compiler II. The design is implemented with a 32 nm technology. Furthermore, we compare the area, power and the critical delay of the M3D integration and a 2D baseline.

Applications of Pattern Matching in Lithography

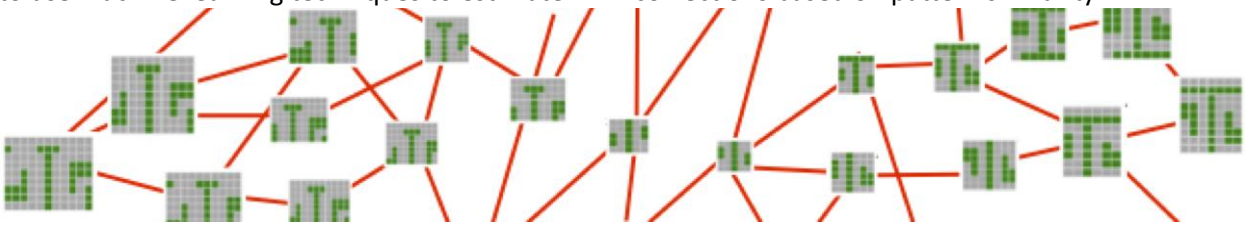
Thomas V. Pistor[a], Rok Yu[a], Luigi Capodieci[b], Vito Dai[b]
[a]Panoramic Technology Inc., [b]Motivo Inc.

Pattern matching algorithms using matrix-based pattern descriptions have many applications in lithography. An implementation of a fast pattern matching algorithm and its script-based interface are described. Well-known examples of pattern matching applications including retargeting, OPC, SRAF-placement and DRC are shown while two fairly recent applications are described in further detail.

A triple-patterning color decomposition algorithm that employs pattern matching to identify polygon break-points and pre-color specific features is described.



Another recent advanced application makes use of the flexible and fast pattern search to build a *pattern coverage tree* that can be used to identify where two layouts differ both from a pattern perspective and from a CD perspective. This approach can be extended as it will be described in an associated presentation, to use machine learning techniques to estimate DFM corrections based on pattern similarity.



Session 4

Presentation Schedule for
Tuesday, November 5, 2019

Session Chairs
Noriaki Nakayamada
Mike Rieger

	Time	Presenter	Title
Session 4	8:00 – 8:50 AM	Winfried Kaiser	***Plenary talk: The Evolution of Lithography Optics: From UV to EUV and beyond***
	8:50 – 9:15 AM	Siva Kanakasabapathy	Title to be announced
	9:15 - 9:40 AM	Andy Neureuther	EUV Lithography Fundamentals: Measurements and Models
	9:40 - 10:05 AM	BG Kim	New approach to EUV solutions for easy access to EUV HVM
	10:05 – 10:35 AM	BREAK	

The Evolution of Lithography Optics: From UV to EUV and beyond

Winfried Kaiser
Carl Zeiss SMT GmbH

For more than 50 years “Moore’s Law” has been driving the steady progress in semiconductor technology resulting in the continuously increasing density and complexity of ICs. These allowed performance gains while functional cost and power needs decreased over many orders of magnitude.

Over decades this “Law” has ruled the development of the lithography optical systems as the heart of the exposure tools, the stepper or scanner, since the optical resolution has become a key enabler for printing smaller features of an electronic device. The classical formula for the resolution of an imaging optics first derived by Ernst Abbe (1873) is

$$Res = k1 \times \lambda / NA$$

(λ is the exposure wavelength, NA the Numerical Aperture of the optical system, k1 the process factor determined by the processing technology including mask, resist and exposure tool with the optics)

Lithography optics has developed from the original blue light (“g-line” with 436nm) to today DUV (“ArF” with 193nm) and to a NA of 1.35 enabled by water immersion allowing a practical resolution of 38nm (hp).

After a long development period the industry today has made the technology step to use EUV (with 13.5nm and NA of 0.33 with a resolution of 13nm for volume production of ICs, definitively the biggest leap in lithography technology ever!

Due to the very short wavelength EUV optics can only work with mirrors in vacuum. The number of mirrors is strictly limited to secure a healthy productivity of the exposure tool. This implies a completely different structure of the optical system compared to DUV optics.

The mask (reticle) is always an optical element as part of the lithography optical system. For EUVL it must be a flat mirror element different to DUV where it is always a transparent glass plate. This causes new effects, most prominently the “Mask 3D Effects” which influence imaging and overlay directly.

While the current generation of EUVL tools are already being used in chip production, the next generation is now in preparation. The optical system for the “High NA EUV” exposure tool will have a NA of 0.55 and a resolution of 8nm for direct printing of the finest features.

Driven by the NA and the higher resolution these optical systems are much larger, the curvatures of the mirror surfaces are more extreme and require an even higher accuracy in the whole manufacturing process which is an enormous challenge especially for the mirror metrology. To produce these systems a completely new manufacturing infrastructure is needed which is currently being build up parallel to the product design and technology development. This enabled the recent production start of the first parts for prototypes.

Title to be announced

Siva Kanakasabapathy

LAM

EUV Lithography Fundamentals: Measurements and Models

Andrew Neureuther, Stuart Sherwin, Luke Long, Jonathan Ma, and Patrick Naulleau

U.C. Berkeley and LBNL

Fundamental EUV measurements and models are described for masks, resist stochastics, radiation chemistry, and dissolution noise. The phase versus angle of "As-Built" multilayer blanks is important both for software pre-compensation OPC, SMO, etc. and tool operation. A simple spectrometer is convenient for characterization but only measures reflectance. Fortunately, causality implies that the phase of the reflection coefficient is related to the magnitude by a Kramer-Kronig type relationship. This related behavior helps in formulating strategies for using a spectrometer to measure and model EUV mask blanks and work is continuing on extensions for characterizing phases in patterned masks.

A 3D reaction diffusion Multivariate Poisson Propagation Model (MPPM) has been developed for investigating chemical gradients and stochastic levels among local concentrations in various resists mechanisms. In addition early exploratory measurements of latent images in novel resist are being conducted by using the wavelength dependence of x-ray scattering near the band edges of various elements.

To further understand radiation chemistry of EUV resists and guide improvements a simulation framework is being developed using available TDDFT and FSSH-MD computational tools. The framework includes the x-ray generation of a photoelectron cascade and excitation of PAG by both low energy photons and electrons. The dominant pathways and key properties that correlate with resist performance are being identified. Measurements of the photoelectron spectrum from resists and substrate coating materials are also being made.

An algebraic model commensurate with case-by-case SEM contact inspection and dissolution simulation is presented for extending missing contact prediction to extreme limits. Local inhomogeneity always exists within a 3D volume of resist and imposes fundamental constraints on lithography such as for reducing missing contacts. Multiple adjacent paths in resist dissolution with local Poisson statistics predict the existence missing contacts at a probability of $2.7\ 10^{-6}$ at 21.8 mJ/cm^3 for 25 nm contacts that agrees with the tail seen in histograms of contact size. Using a finite covering technique shows the probability scales slower than Gaussian and yet falls to 10^{-15} at 40 mJ/cm^3. The stochastic Multivariate Poisson Propagation Model (MPPM) is used to examine the nature of inhomogeneity in resists and the role of image quality.

This research is sponsored by C-DEN (Center for design-enable nanofabrication). Member companies ASML, Carl Zeiss Group, Intel, KLA-Tencor, and Mentor Graphics, This work was performed in part at Lawrence Berkeley National Laboratory which is operated under the auspices of the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

New approach to EUV solutions for easy access to EUV HVM

Byung Gook Kim, Dong Gun Lee

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bgkim@euvsol.com

EUV lithography has started to enter its volume production from N7 logic device. However, the current infrastructures such as EUV metrology, inspection, resist and pellicle for EUV mask and EUV lithography still need to be improved for high volume EUV production. Furthermore, the burdensome to access and equip the high cost EUV related tool make slow down EUV proliferation. To solve these requirement, ESOL has developed high reliable and simple HHG EUV source and applied its application from EUV metrology to EUV material development area. In this presentation, ESOL will suggest efficient way of thinking to make anyone can access EUV with ease and low cost.

Keywords: low cost EUV solution, HHG EUV source, EUV metrology, EUV inspection, EUV material development.

Session 5

Presentation Schedule for
Tuesday, November 5, 2019

Session Chairs
Danping Peng
Ravi Mahajan

	Time	Presenter	Title
Session 5	10:35 – 11:00 AM	Robert Bristol	High-NA stochastics: a method for making practical progress today
	11:00 – 11:25 AM	Linyong Pang	Making Digital Twins using the Deep Learning Kit (DLK)
	11:25 – 11:50 AM	Stephen Renwick	193nm lithography's path to the future
	11:50 AM – 12:15 PM	Andreas Olofsson	Title to be announced
	12:15 - 12:40 PM	Oliver Patterson	An In-Line Test Structure Approach for Quantifying Edge Placement Error
	12:40 - 1:05 PM	Andreas Erdmann	Perspectives & tradeoffs of novel absorbers for EUV lithography
	1:05 PM	End Session	

High-NA stochastics: a method for making practical progress today

Robert Bristol

Intel Corporation

Abstract: As we scale down to ever-smaller feature sizes, the corresponding limits to the Edge-Placement Error (EPE) budget become increasingly severe. Improvements in the litho tool (better aerial image, more photons) will help, but eventually resist stochastics may become the limiting factor, especially as we move towards the sub-20nm feature sizes achievable with high-NA EUV. But it is not straightforward to make progress today on materials intended for tools which do not yet exist. Research-type tools can be used to demonstrate the ability of a resist to resolve small features, but typically only on relatively small population sizes. A few organizations have access to production-worthy EUV scanners and can generate data on large populations with good stability, but only for relatively large features and with limited bandwidth for experimental materials. This paper argues why either approach alone is likely insufficient and may lead to material dead-ends, e.g. the best stochastic material for large features may fundamentally not be the best for smaller ones. Instead, we propose a hybrid method to combine key data from both research lithography tools (ebeam and micro-field EUV) with today's production EUV scanners.

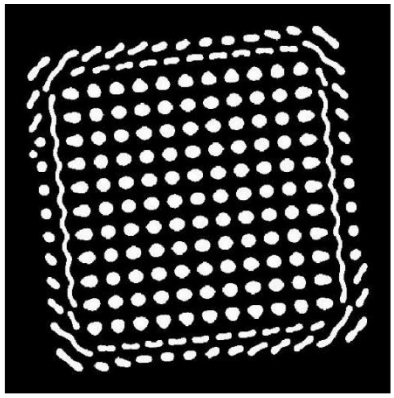
Making Digital Twins using the Deep Learning Kit (DLK)

Linyong (Leo) Pang
D2S, Inc.

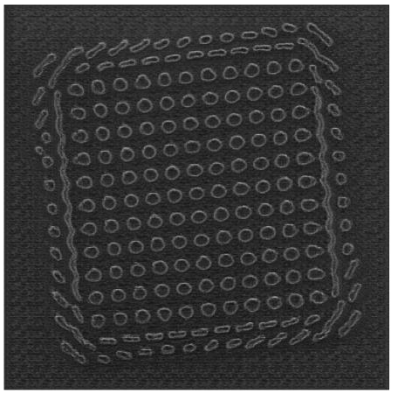
Deep Learning (DL) is one of the most exciting fields in AI right now. It's still early days, but DL will totally change the lithography and photomask industry to automate or optimize the efficiency of equipment and processes. The key element required for building applied DL is a GPU-accelerated simulation environment, which can be used to build "digital twins" of real world equipment and process. In this paper, we will present a DL Starter Kit – including the simulation platform, what it can do, why you need it, and show you the latest examples how you can use it to solve lithography and photomask problems.

Deep learning requires a very high volume of "trial and error" episodes — or interactions with an environment — to learn a good policy. Therefore simulators are required to achieve results in a cost-effective and timely way. Just imagine trying to teach a hot spot detection tool to detect hot spots in design by throwing millions of designs to tape out, write masks, process it, print wafer with scanners, process it, then measure millions of locations on SEM. Simulators allow these episodes to happen in a digital world, training an AI-based solution to reach its full potential while saving time and money.

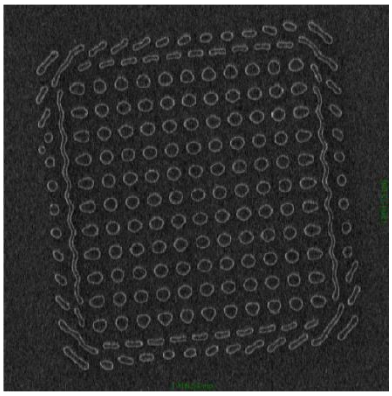
The DL Starter Kit is an artificial intelligence platform that allows semiconductor manufacturing companies and mask shops to do such simulations for deep learning training. The DL Starter Kit provides accurate physical models for mask and lithography that are fully accelerated by CUDA on GPUs, the de facto DL training platform, and is integrated with Tensorflow, the most popular DL framework, and pre-trained neural networks trained for common mask and wafer problems. Using this DL Starter Kit, semiconductor manufacturing companies and mask shops can build digitals twins of their equipment and process: they can leverage pre-trained neural networks to build their deep neural network model, connect the simulator of their choice (either provided by the DL Starter Kit or authorized partner's GPU accelerated simulators), and train the neural network model in that environment to learn a desired behavior.



Simulated Mask Pattern



SEM image by Digital Twin



Real SEM image

193nm lithography's path to the future

Steve Renwick and Donis Flagello
Nikon Research Corp. of America

Several years ago, the question asked at conferences and forums was basically, "193 immersion or EUV?" The unspoken assumption was that one lithographic technology would dominate leading-edge lithography. That was oversimplified. Rather than following a neat and predictable scaling path, lithography has fragmented into a multiplicity of options: EUV, nano-imprint litho, 193i multiple patterning, and others. Each has its advantages (EUV's high resolution, 193i's low cost) and disadvantages (EUV's stochastic errors and line-edge roughness, 193i's resolution limit). Relative costs are infrequently assessed and depend on the particular application.

Meanwhile, one manufacturer is developing a new option: DUV maskless lithography. This presents an interesting alternative for prototyping, chip development, and other applications that need frequent mask design changes. Of course, it raises a whole set of new challenges. Are there different resolution limits? Does the cost savings of having no mask really make it worth the trouble?

This talk will examine the different options available, citing the pros and cons of each, and show both lithographic and cost analyses, with some surprising results.

Title to be announced

Andreas Olofsson
DARPA

An In-Line Test Structure Approach for Quantifying Edge Placement Error

Cyrus Tabery, Oliver D. Patterson
ASML, San Jose, CA

Shrinking integrated circuit feature dimensions has been the dominate path of progress in the semiconductor industry over it's 50 year history. Impressive improvements in component process capability, including lithography, etch, deposition and planarization, have made this possible. At the same time, major advances in inspection and measurement technique, have provided a way to develop and monitor these processes in a timely manner. Recently process margins have become so tight that edge placement error (EPE) has become a hot topic at lithography conferences. Thorough exploration of alternate ways of characterizing EPE and process margins in general could prove very useful for the industry as a whole.

This presentation discusses exploratory work in the use of in-line voltage contrast test structures, in the form of design skews, for characterizing edge placement error and critical process margins. This approach is compared to alternative in-line approaches to highlight its advantages. These structures are inspected after metal CMP and therefore have the advantage of capturing the impact of all process steps (deposition, lithography, etch and CMP) in the module. Because they use voltage contrast, 100% capture of both buried and surface defects is possible, while nuisance defects are inherently filtered out. Using electron flow rather than electron or photon surface emission to measure the proximity of neighboring feature edges potentially is much more accurate and factors in the impact of line edge roughness. Results will be presented on the latest simulated and experimental verification of these test structures.

Perspectives & tradeoffs of novel absorbers for EUV lithography

Andreas Erdmann, Hazem Mesilhy, Peter Evanschitzky
Fraunhofer IISB, Erlangen, Germany

Present masks for EUV lithography employ tantalum based absorbers with a thickness of about 60 nm on top of a reflective multilayer. The large ratio between the absorber thickness and the wavelength, the reflective multilayer and the oblique illumination of the mask cause mask 3D effects. The new anamorphic optics of NA=0.55 systems introduces several additional mask 3D related imaging artefacts. We employ various physical models to study the root causes and characteristics of related mask 3D effects and to explore the performance of alternative absorber materials.

Figure 1 presents a schematic view of an EUV mask that highlights the role of the absorber pattern, of the reflective multilayer and of the resulting multiple diffraction effects. The diffracted light in the projection lens is formed by superposition of multiple individual diffraction orders of downward and upward propagating light. It depends both on the physical properties (thickness, extinction coefficient k, refractive index n) of the absorber and on the distance between a virtual absorber diffraction plane and a virtual multilayer reflection plane. Hybrid mask models are employed for a quantitative investigation of the related imaging effects.

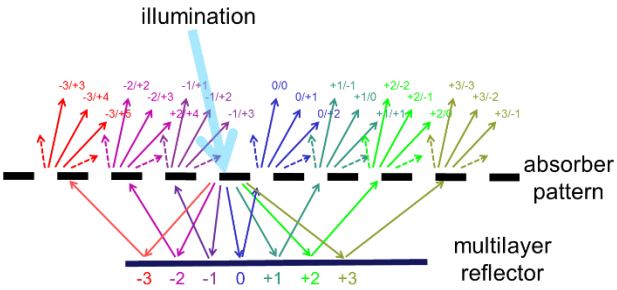


Figure 1: Double diffraction scheme for EUV masks. Thick downward arrow: incident light; other arrows: orders which are created by diffraction from the absorber (thick horizontal dashed line) and reflection from the (multilayer) mirror (thick horizontal solid line).

Alternative absorber materials can provide an improved balancing of diffraction effects and better imaging performance. However, the best solutions present a tradeoff between different lithography metrics including high NILS, low nTC and high threshold-to-size (THRS). Multi-objective optimization techniques were used to explore this tradeoff. Figure 2 shows typical computed Pareto data for different absorber materials. Simulations of various use cases and material options indicate two main types of solutions: high k materials (k>0.05, especially for vertical lines/spaces) and low n materials (n ~ 0.9) to provide phase shift mask solutions.

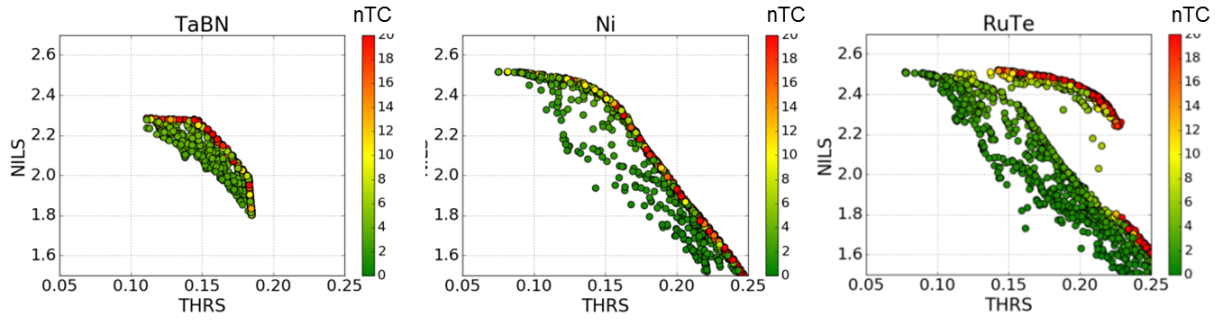


Figure 2: Simulated Pareto data for different absorber types/materials and vertical trenches at the edge of the exposure silt and variable illumination.

Session 6

Presentation Schedule for
Tuesday, November 5, 2019

Session Chairs
Mike Meyer
Martin Burkhardt

	Time	Presenter	Title
Session 6	7:00 – 7:25 PM	David Fried	Technology Node Scaling Through Variation Control
	7:25 – 7:50 PM	James Shiely	Found in Translation
	7:50 – 8:15 PM	Stephen Hsu	EUV Imaging optimization to reduce the impact of wavefront aberrations
	8:15 – 8:40 PM	Vidya Vaenkatesan	Local Errors on EUV Mask and its Impact on Wafer
	8:40 – 9:05 PM	Ivan Ciofi	Calibrated Modeling of Line-to-Line Dielectric Reliability: LER Specs to Meet Reliability Constraints at Operating Conditions
	9:05 – 9:30 PM	David Chanemougame	Agile PPAC platform for fast exploratory DTCO: the LGAA CFET case
	9:30 - 9:55 PM	Nelson Felix	The Evolution of Patterning Challenges from High-Performance Computing to AI Applications
	9:55 PM	End Session	

Technology Node Scaling Through Variation Control

David M. Fried, PhD
Lam Research Corporation – Computational Products

While lithography has borne the burden of executing technology scaling, every device generation has been built upon fundamental process, device and integration innovations. For example, the development of Rapid Thermal Anneal (RTA) processes facilitated high dopant activation and more abrupt device junctions, leading to closer packing of transistor source/gate/drain terminals. The FinFET, a double-gated fully-depleted transistor structure, has delivered improved electrostatic control and allowed scaling to continue through use of shorter gate lengths. Even NAND Flash has seen fundamental innovation, with the transition from planar 2D to multi-layer 3D devices, which has led to increased device density and "More than Moore" scaling.

Today, the list of these fundamental technology scaling innovations seems to be running thin. Perhaps Gate-All-Around (GAA) structures will further advance gate length scaling, or 3D geometries like C-FETs will deliver increased logic device density as seen in the transition from 2D to 3D NAND Flash. However, the single largest opportunity for scaling advantage may lie in an area rarely viewed as "fundamental innovation". Process and structural variations, or tolerances, have become a larger and larger component of dimensional scaling. A substantial reduction in these variations, or the impact of these variations, may be the greatest available path to technology scaling today. The reduction of process variation has typically taken place as technology moves into high-volume manufacturing, not during technology development. Taking advantage of this opportunity will require a significant shift in how technology development occurs. In this discussion, we will examine how process variation fits into the definition of technology scaling and why process variation is starting to dominate scaling dynamics. Next, we will review opportunities for technology scaling purely through variation reduction, using novel processes, integration schemes and most importantly active process control. Finally, we will discuss how technology development must change to take advantage of these additional technology scaling opportunities.

Found in Translation

James P. Shiely [1]
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The microlithography system can be modeled as a communication mechanism. The purpose is to transmit a message representing a design through thechannel of a scanner and onto the wafer. During transmission noise corrupts the message. The photo mask encodes the mask data to optimize robustness of the message to corruption by noise.

Viewed in this context, the flow of data is a sequence of translations: from design to mask. From mask to aerial image. From aerial image to post-resist or post-etch wafer contour.

Deep learning has advanced the accuracy and speed of natural language translation. This is often achieved by encoding text in one language as a lower dimensional embedding, and decoding the text into a different language. It is then necessary to learn either a mapping between embeddings or a shared representation in order to effect the translation.

The purpose of this work is to evaluate whether benefit is observed in extending this insight from natural language processing into microlithography.

The method of the work will be to evaluate a resist modeling neural net-works learning efficiency, holding the training data constant but varying neural architecture and training methodology. We will specifically evaluate learning efficiency of conventional Deep Neural Network architectures in comparison to neural architectures and training methods inspired by neural machine translation.

EUV Imaging optimization to reduce the impact of wavefront aberrations

Stephen Hsu
ASML Brion, San Jose, CA

Chipmaker started to adopt extreme ultraviolet lithography (EUVL) in volume manufacturing in 2018 for sub-7nm node critical device layers. The wavelength of EUV is an order of magnitude smaller than ArF, for the same optics surface error the wavefront errors increases significantly. There are two synergic steps to reduce the aberration sensitivity: Source mask optimization (SMO), and wavefont optimization (WFO). The first the is to optimize a pupil to reduce the aberrations sensitivity of critical patterns and to meet the imaging contrast requirement. The second step is per-scanner wavefront optimization for reducing the tool-to-tool CD and CD asymmetric difference on the critical patterns selected from a full-chip. The Source mask optimization and wavefont optimization needs to work together to maximize the imaging and scanner matching performance for a specific device layer.

Reducing the CD through-slit and across field on critical device patterns between scanners are very critical as part to the total edge placement errors(EPE) budget. In high volume manufacturing, in order for chipmakers to increase the scanner productivity, reduce the cost of making multiple copies of reticle, and maximize the operational flexibility in the fab, the same reticle need to be shared amongst the qualified scanners. With the these requirements, ASML developed ImageTuner-NXE product to provide the layer specific scanner wavefront optimization capability to improve the matching performance within customer's specification.

The wavefront optimization adopts the edge placement errors (EPE) as the cost function to minimize the through-slit EPE difference between the reference and to-be-matched scanner. The wavefront optimization flow includes the NXE scanner's lens model to convert the optimized wavefront variables into a scanner mirrors positions in the projection optics and the final output is a total set wavefront in the form of scanner sub-recipe which can be directly accepted by the to-be-match scanner. With no additional wavefront manipulator, the wavefront correction capabilities and through-slit matching for a specific device layer is a big challenge. The setup of projection optics box (POB) of an EUV scanner is designed to minimize the total wavefont root-mean-square (RMS) error across the entire mirror surfaces, while the layer specific wavefront optimization minimize the wavefront RMS in the regions of the pupil use for imaging. Therefore, the optimized wavefont gives a better matching performance that cannot be achieved by the standard POB setup procedure.

It is worth noting that conventionally for scanner matching, a "golden scanner" is selected as the reference scanner, and all other scanners matching to the "golden scanner". The drawback of this matching approach is that "golden scanner" lens fingerer print could change due to a lens re-setup which impacts the stability of Work-in-process (WIP) in the wafer fab. A better approach is to use a "aberration free ideal scanner" as the reference scanner, this is a "matching to ideal" strategy and the benefit of such strategy is the ideal machine is a time-invariant, fab independent reference. The rigid body wavefront correction potential is the same for each NXE 3400B scanner, "matching to idea" optimizes each scanner to give the best performance and the tool-to-tool through-slit EPE variation naturally decreases across the entire scanner fleet. We use ASML's LMC+ image based verification to qualify the benefit of WFO results for full chip prior to wafer validation. Case study results show that Source mask optimization and wavefont optimization can effectively reduce the impact of wavefront error and improve the scanner matching performance.

Keywords: Extreme ultraviolet lithography (EUVL), edge placement errors (EPE), pattern placement error (PPE), Aberrations, Source mask optimization (SMO), wavefont optimization ,scanner matching

Local Errors on EUV Mask and its Impact on Wafer

Vidya Vaenkatesan[1], Paul van Adrichem[1], Laurens de Winter[1], Steffen Steinert[2], Dirk Beyer[2], Thomas Scheruebl[2], Renzo Capelli[3]

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[3]Carl Zeiss SMT GmbH, Rudolf-Eber-Str. 2, 73447 Oberkochen, Germany

Overlay (OV), Optical Proximity Correction (OPC), Critical Dimension Uniformity (CDU) budgets are being continually scaled in order to create room for the patterning critical budget Edge Placement Error (EPE)[1]. Mask is a known contributor to intra-field fingerprints at the wafer level impacting OV, OPC and CDU. In a previous study, we have shown mask to contribute to wafer local CD (LCDU) and Placement distribution (LPE)[2] which from Figure 1 can be seen is a sub contributor to the Local CD errors.

Figure 1. Representation of contributors and sub-contributors to EPE budget.

In this work we extend our investigation of mask local placement and CD errors to understand further any mask induced systematics at smaller spatial scales. Dense local registration measurements on mask indicate LPE range of > 4nm and presence of systematic fingerprints (Figure 2). This would translate as a pattern placement error of ~ 1 nm on wafer (single layer). Ramification of mask LPE on OV and subsequent budgets will be discussed. Whilst there are solutions to mitigate mask LPE (e.g., multi beam mask writers), it clearly is a metric of relevance and needs monitoring and control. The ecosystem for addressing mask local errors will be discussed.

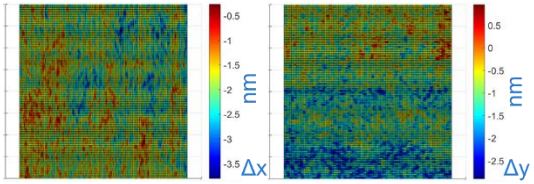


Figure 2. Dense local registration X/Y of 26x16 µm contact array (16261 registration measurements).

Additionally, experimental and simulations data will be used to demonstrate the transfer of mask local variations on wafer.

References

[1] Jan Mulkens *et. al.*, "Holistic approach for Overlay and Edge Placement Error to meet the 5 nm Technology Node requirements", Proceedings SPIE. 10585, (2018).

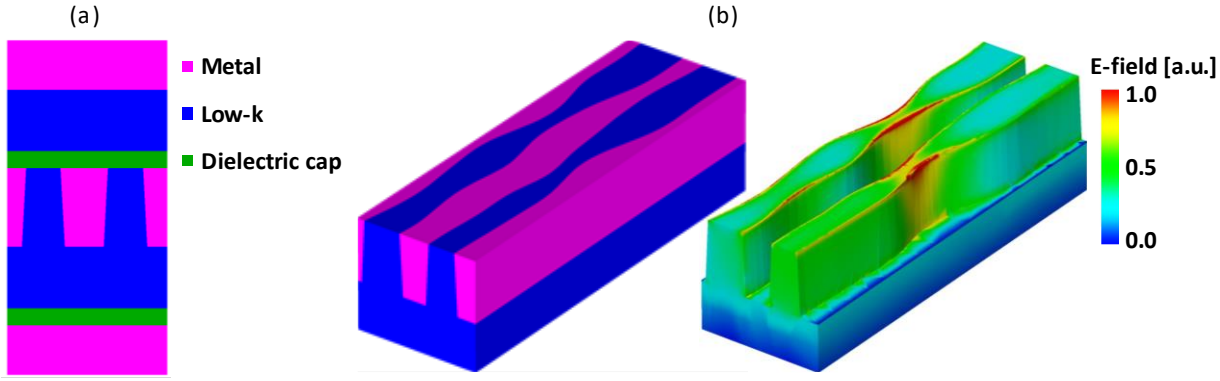
[2] V. Vaenkatesan *et. al.*, **"**Evaluation of local CD and placement distribution on EUV mask and its impact on wafer**"**, Proc. SPIE. 11178, Photomask Japan 2019.

Calibrated Modeling of Line-to-Line Dielectric Reliability: LER Specs to Meet Reliability Constraints at Operating Conditions

Ivan Ciofi[1*], Philippe J. Roussel[1], Yves Saad[2], Lawrence Melvin[2],
Christopher J. Wilson[1] and Kristof Croes[1]
[1]Imec Belgium ([*]Ivan.Ciofi@imec.be), [2]Synopsys

In order to sustain the demanded increase of device density per chip from one technology node to the other, the interconnect pitch has aggressively scaled down in recent years. In contrast, the power-supply voltage (V_{DD}) has not decreased significantly. In addition, litho-patterning variations, such as line-edge roughness (LER) or die-to-die spacing variations, have not reduced much with scaling. Consequently, the electric field that the interconnect dielectrics need to withstand at operating conditions has increased considerably. At the same time, intrametal dielectrics have become weaker, because of the introduction of low-k materials to lower line-to-line capacitance. As a result, the reliability margin has degraded dramatically and nowadays serious concerns are raised regarding future technology nodes. In this respect, predictive models are being intensively sought to enable early assessments of interconnect materials and processes at scaled dimensions.

In this talk, we present our statistical model for line-to-line dielectric reliability predictions at scaled interconnect dimensions. Our model accounts for the location dependence of the electric field (E-field) within the dielectric in-between and along the lines, caused by LER and die-to-die spacing variations (see figure). Besides, our model is calibrated to internal reliability data from Time-Dependent Dielectric Breakdown (TDDB) measurements to enable realistic predictions. We report LER specs to meet reliability constraints as a function of line-to-line spacing and related die-to-die variations for interconnect dimensions ranging from 16nm to 8nm half-pitch. Finally, we elaborate on our predictions for various litho-patterning approaches, including EUV Single Patterning (SP) or Self-Aligned Double Patterning (SADP), 193i Self-Aligned Quadruple Patterning (SAQP) or Self-Aligned Octuple Patterning (SAOP).



Mapping of the electric field (b) within the intermetal dielectric of typical Cu/Low-k interconnects (a), as obtained from 3D simulations in Sentaurus (Synopsys). The electric field within the dielectric changes both across and along the lines (b).

Agile PPAC platform for fast exploratory DTCO: the LGAA CFET case

D. Chanemougame[1], L. Liebmann[1], J. Smith[1], J. Cobb[2], P. Asenov[3], M. Berkens[4], M. Choi[2], V. Moroz[2], H. Wheeler[2], R. Borges[2] and A. DeVilliers[1]
[1]TEL Technology Center, Albany, NY, USA, [2]Synopsys, Inc., USA, [3]Synopsys, UK,
[4]SAGE Design Automation, Eindhoven, Netherlands

Today's leading-edge is nothing except the steady, consistent accumulation of learning and incremental changes, node after node. But 50% area scaling while still achieving the traditional power and performance gains is harder than ever. Engineers are increasingly feeling the effects of long-dreaded fundamental limits of physics and stochastics for devices, interconnects and materials. This is not so much a solid wall, more of a foggy, thick and sticky mud trail surrounded by cliffs. Innovations in processes, device architectures and designs, can provide significant advancements, but invariably come with a rapid rise of complexity and cost. Not to forget unfamiliar risk levels. How to navigate through so many options at all major levels, and still achieve relevant power-performance-area-cost (PPAC)? The process-design-kit (PDK) is the industry standard used to efficiently and accurately model a technology PPAC by ways of simulations. A large collection of interlinked software elements, from device TCAD & spice modeling, design rules checkers (& hardware validation), RC parasitics extraction etc., the PDK is very capable, and by definition, extremely specific and rigid. Change anything in the technology, and very likely it won't be able to handle it. To build a PDK is an intense, multiple-months effort, involving multiple areas of expertise from large design enablement teams. As such, not only selecting the wrong technology definition is possible, but critical issues will finally be exposed many months after major technology choices are solidly locked in. R&D engineers painfully realized they must engage much earlier together, from process, integration & patterning to device and standard cells, all the way to designers. This realization is DTCO: identify the right needs and roadblocks, and develop viable solutions early enough. However, reaching relevant PPAC beyond 3nm requires to combine a much higher level of disruptions on all fronts. Significant PPAC interactions can be expected, and DTCO efforts must scale up and accelerate to test large numbers of combinations. With adequate, yet rigorous electrical modeling and circuit simulations, comprehensive documentation can be established. Variability and the system's sensitivity to it should be included, as designers are forced to be more conservative, shaving up the performance envelope.

In this discussion, we will present such an agile, automated PPAC platform, capable of fast exploratory DTCO and meaningful technology prototyping. We will show how any core technology definition can be built and assessed, with any combinations of device architecture and process integration. Similarly, various scaling propositions based on logic standard cell libraries can be evaluated. Benchmarking an N3-like CFET to a probable N3 finFET reference, we will then present how the 1st stage of rigorous PPAC analyses can be done at the standard cell level. By generating a circuit netlist without a full design enablement effort and a PDK, but with much faster turn-around time, many more iterations with a wide experimental variety can be enabled, opening up the way to library characterization and the 2nd more advanced stage: block-level PPAC.

The Evolution of Patterning Challenges from High-Performance Computing to AI Applications

Nelson M. Felix, Ph.D.
IBM Semiconductor Research, Albany, NY

EUV patterning represents an extreme version of many of the patterning challenges that have faced logic scaling for decades. However, it remains one of the key enablers to delivering robust semiconductor node scaling, due to its ability to deliver high-fidelity patterns with a single exposure, in comparison to lower fidelity multi-patterning techniques previously employed by the semiconductor industry at the 14nm node and below. As transistor scaling slows, interconnect scaling driven by EUV is key to enable continued advances in logic computing performance. Concurrently, new transistor types are being enabled directly by EUV patterning and driving unique requirements not seen to date. At the same time, the requirements for AI hardware development represent a new set of challenges complementary to those faced in logic hardware development.

We will review the current state of patterning challenges for logic scaling and discuss what drives new patterning challenges related to AI hardware.

Session 7

Presentation Schedule for
Wednesday, November 6, 2019

Session Chairs
Thomas Scherübl
Anton Devilliers

	Time	Presenter	Title
Session 7	8:00 – 8:50 AM	Ravi Mahajan	***Plenary Talk: Advanced Packaging Architectures for Heterogeneous Integration***
	8:50 – 9:15 AM	Chris Progler	Is perfection the new standard for functionally matched photomasks?
	9:15 – 9:40 AM	Ingo Schulmeyer	Corrected Low Voltage SEM for Metrology and Analytics
	9:40 - 10:05 AM	Michael Yeung	Use of GPU accelerated Maxwell solver in rigorous lithography simulation
	10:05 – 10:35 AM	BREAK	

Advanced Packaging Architectures for Heterogeneous Integration

Ravi Mahajan, Kemal Aygun, Zhiguo Qian
Intel Corporation

Advanced packaging technologies have risen in prominence because of their value as key compact, power efficient platforms for heterogeneous integration (HI) needed to meet increasing computing performance demands. This talk will focus on mainly on interconnect capabilities available today and projections for their continued evolution. Different packaging architectures will be compared primarily on the basis of their physical interconnect capabilities. Key features in leading edge 2D and 3D technologies, such as EMIB, Silicon Interposer, Foveros and Co-EMIB will be described and a roadmap for their evolution will be presented. The talk will conclude with a discussion of opportunities and challenges in driving the package roadmap forward.

Preferred file naming convention is author's-last-name_paper-title.doc or author's-last-name_paper-title.docx

Is perfection the new standard for functionally matched photomasks?

Chris Progler
Photronics Inc., Allen, Texas

As the first physical realization of design intent, the photomask is critical for IC time to market, design portability, adoption rate and production fan out. Therefore, the ability to rapidly produce and verify photomasks with a functional performance matching the one developed during original process setup can be enabling for these aspects of chip production. While functional mask matching may appear at first to be a routine matter, for advanced processes in particular even the ability to determine if two masks will behave in optically identical ways under a given imaging application can be problematic. From nanometer class signature matching to design dependent hot spots with complex mask-wafer imaging characteristics, the notion of what it means to produce a functionally matched mask has grown more abstract. This is especially so when one considers typical design to design layout variations within a given process family and the higher standard on chip security and reliability. Building each mask to formal specification and keeping design layout within guard banded mask rule checks (MRC) helps but does not always ensure new design success within a qualified process. Expanding mask specs and rules to address this issue results in a tradeoff between rule driven layout inflexibility and spec driven mask first pass yield (FPY). FPY in particular directly impacts mask cycle time which appears more and more to be the most critical mask performance metric across nodes and applications as it impacts time to market and design wins. Of course, the problem becomes manageable with abundant time to verify the functional matching of a mask to a previously built mask but such time is not always available. That is, the mask must be built very fast and it must function as expected with robustness to new design variability.

Example use cases for functionally matched masks range from building first time right masks for new designs within a qualified process node to simply building a new mask to replace a retired mask in production. A careful understanding of matched masks is also required to expand mask output under existing processes of record or to facilitate simplification or upgrade of lithography production processes. When considering advanced processes such as multiple patterning and EUV, we find the challenge of ensuring functionally matched masks to be compounded due to stronger inter-mask effects and the interaction of the mask with the wafer imaging viewed against tight wafer process margins.

We will review some of the background, requirements and observations associated with building functionally equivalent masks for a few different applications and nodes and highlight characterization methods developed to support functional mask matching. Data methods such as process simulation and mask process correction come into play along with methods to flag excursions in both process and layout that can warn us about the manufacture of a mask not meeting functional equivalence requirements. Finally, we will consider some future developments that might improve the success ratio and convergence speed on producing functionally matched masks which can have a major impact on IC design to volume production.

Corrected Low Voltage SEM for Metrology and Analytics

Ingo Schulmeyer, Daniel Fischer
Carl Zeiss SMT, Process Control Solutions

Shrinking feature sizes and the use of materials more sensitive to e-beam damage are making the use of conventional Scanning Electron Microscope (SEM) technologies more challenging and in some cases just not possible. One problem is, that the improvement in SEM resolution is not keeping pace anymore with the scaling of design nodes. Another factor is, that the e-beam radiation causes sample damage, e.g. shrinkage in resist. To avoid that, there is a requirement to go to smaller landing energies while maintaining high resolution to reduce the damage to a minimum. Another requirement that is becoming more important in SEM is to add analytical information on the different materials on a given sample. This allows a better understanding of material distribution and the nature of defects.

In this paper we introduce a novel SEM, capable of correcting the spherical and chromatic aberration of the lens. This allows extremely good resolution especially at low landing energies. We achieve sub nm resolution down to 50eV. In a first case study we evaluate and quantify the resist shrinkage at different landing energies and demonstrate the advantage of going to lower voltages. We also discuss how surface sensitivity and image quality changing its properties when going to ultra-low landing energies. In a second case study we show, how the contrast formation of backscattered electrons (BSE) can be used to differentiate different materials and enable analytics on a nm scale.

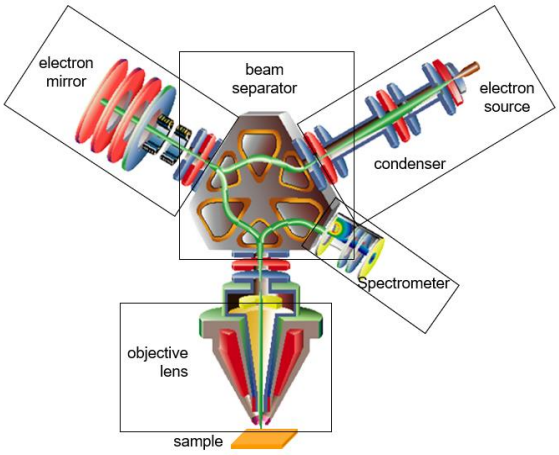


Figure 1: Schematic of the main components of the DeltaSEM column

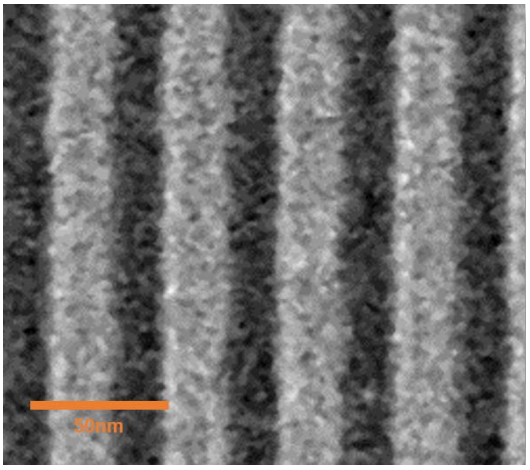


Figure 2: EUV CAR resist lines revealing also surface morphology, imaged at 70eV

Use of GPU accelerated Maxwell solver in rigorous lithography simulation

Michael Yeung
Fastlitho, San Jose, CA, U. S. A.

We first present an eigenvalue analysis of our new pseudo-spectral time-domain (PSTD) formulation for curvilinear coordinates introduced recently in [1]. This analysis (see Fig. 1) demonstrates beyond any doubt that our new PSTD formulation is numerically stable for rigorous lithography simulation involving complicated curvilinear mask geometries.

We then apply our new Maxwell solver to rigorous simulations involving real, as opposed to ideal, mask structures containing both line-edge and surface roughness (see Fig. 2). Such simulation involving realistic-looking mask structures is important for accurately assessing the impact of various types of mask imperfection on the wafer image.

Next, we address the issue of speed in lithography simulation. We explain, by using the example of two-dimensional fast Fourier transform (FFT), which is the bread-and-butter algorithm of most lithography simulation tools, why the GPU is an ideal platform for accelerating lithography simulation. Benchmarks are given to compare the performance of 2D FFT on the GPU and CPU platforms for lithography simulation.

Since the GPU usually has rather limited memory, in order to use it for large-area lithography simulation, a multiple-GPU approach is needed. Here, a large simulation domain is divided into smaller domains which can fit into individual GPU's on a single motherboard. During each step of the computation, information is passed between the GPU's to enable the algorithm to advance. We present benchmarks to demonstrate the multiple-GPU approach for large-area rigorous lithography simulation.

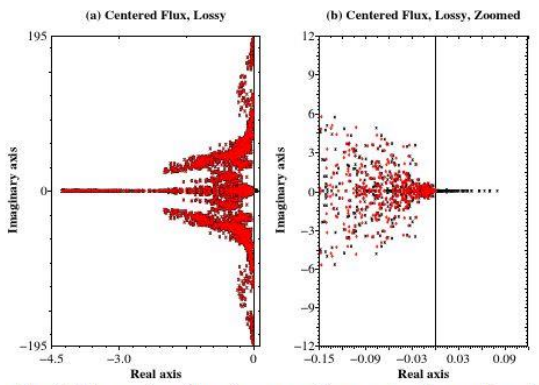


Fig. 1. Eigenvalues for a lossy scatterer using the centered flux scheme. Red: New PSTD formulation. Black: Old PSTD formulation.

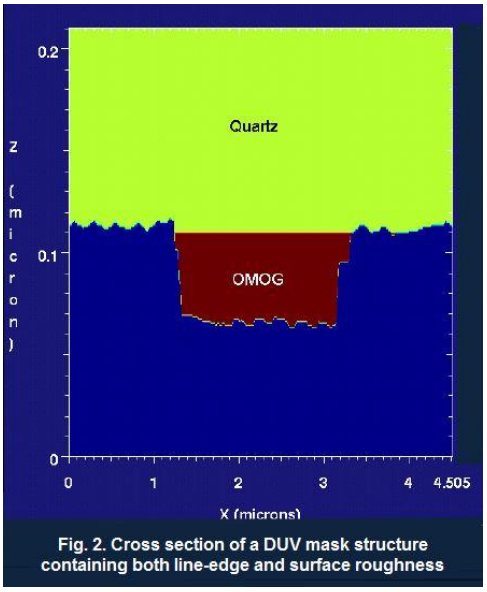


Fig. 2. Cross section of a DUV mask structure containing both line-edge and surface roughness

[1] M. Yeung and E. Barouch, "Development of fast rigorous simulator for large-area DUV and EUV lithography simulation", presented at SPIE Advanced Lithography 2019.

Session 8

Presentation Schedule for
Wednesday, November 6, 2019

Session Chairs
Pat Martin
Jeff Smith

	Time	Presenter	Title
Session 8	10:35 – 11:00 AM	Andrey Rudenkow	Unexpected Challenges in Material Quality at the Leading Edge
	11:00 – 11:25 AM	Samee Rehman	Optimizing Overlay using Machine Learning on Fab Context Data
	11:25 – 11:50 AM	Tetsuro Nakasugi	The future of NIL: enabling a new semiconductor manufacturing
	11:50 AM – 12:15 PM	Mike Green	Advanced modeling techniques for mask process development and verification
	12:15 – 12:40 PM	Brian Cline	DTCO in 2019: The Precious Metal Stack and the Route to Better Designs
	12:40 - 1:05 PM	Curtis Zwenger	Challenges Facing Photolithography in Advanced Packages
	1:05 PM	End Session	

Unexpected Challenges in Material Quality at the Leading Edge

Dr. Andrey Rudenko
Dow Chemical

With IC fabrication becoming ever more complex, suppliers of electronic materials face new challenges with regard to the purity of the raw materials, cleanliness of manufacturing equipment and analytical capabilities in order to meet the requirements of the semiconductor industry. For the most advanced nodes, much of the focus has been on metallic impurities, with the industry now demanding values in the double-digit part-per-trillion range per metal. Less attention has been paid to organic impurities. We will present some case studies demonstrating the impact of organic impurities in the low ppm range and the challenges these impurities pose from a raw material supply chain, detection and process control perspective.

Optimizing Overlay using Machine Learning on Fab Context Data

Samee Ur Rehman
ASML, San Jose, California, USA

LithoInSight (LIS), an ASML application product, has proven to improve the ability of advanced process control in overlay with accurate fingerprint estimation and optimized scanner correction. It is now often taken as Process of Record (PoR) for performing chuck/lot based HVM run-to-run control among advanced semiconductor manufacturers. In order to further improve the On-Product Overlay (OPO) performance given the shrinking node size, the question of how to effectively combine lithography and non-lithography data has been asked frequently. In this presentation, we will show how machine learning can effectively leverage data coming from process contexts (e.g. process context information) together with overlay metrology in order to improve OPO.

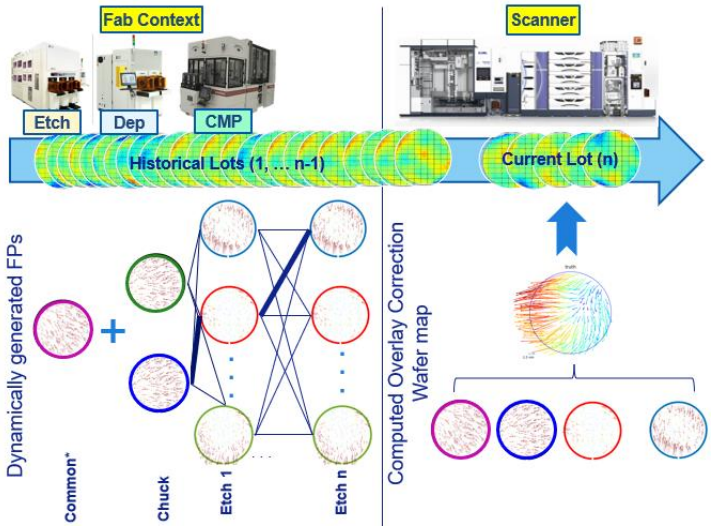


Figure 1: A machine learning model is used to dynamically learn an overlay fingerprint per context given ID of the contexts along a wafer route as well as overlay data from previous lots.

The machine learning model (Figure 1) takes as input categorical data, such as the ID of the different process tools along a wafer route, together with overlay data from previous lots for the current layer, in order to learn decomposed overlay fingerprints per fab context. The fingerprints predicted by this machine learning model are then used for correction inside run-to-run control.

In this conference we will present our results to date. Using synthetic data, we will show that the fingerprints corresponding to different contexts can accurately be predicted via the proposed methodology. The OPO performance of the novel run-to-run control with the integrated machine learning model will then be compared to POR on experimental data. Finally, we will also study the tradeoff between improving OPO and increasing overlay metrology via rigorous Monte Carlo wafer sampling analysis.

The future of NIL: enabling a new semiconductor manufacturing

Tetsuro Nakasugi
Process Technology Research & Development Center,
Institute of memory technology Research & Development,
Toshiba Memory Corporation

The challenges of nanoimprint lithography (NIL) are overlay, defects, throughput, template life, and the fabrication of template. The overlay and defects must satisfy the requirements of the products applied. The throughput needs to provide adequate cost of ownership (CoO). Since NIL is a contact process, template damage by the particles on a wafer is inescapable and a longer template life is required for mass production. The defect-free template having 1x-nm feature size is also needed. In general, patterning of high resolution template can be performed by electron beam (EB) lithography. But, insufficient resolution of EB resist poses a risk of defect generation. These challenges of NIL are sufficient to divert attention of most of the lithographers away from NIL.

However, we are coming to the place to overcome these challenges by the progress of NIL system, process technology and template manufacturing technology. We have developed a nanoimprint lithography (NIL) technology including NIL system, template and resist process for half pitch (hp) 14 nm direct pattering. The latest NIL system NZ2C shows the mix and match overlay (MMO) of 3.4 nm (3σ) and the template life around 340 lots. Throughput of 80 wafers per hour (wph) has been demonstrated using throughput enhancement solutions, such as gas permeable spin-on-carbon (GP-SOC) and multi field dispense (MFD). The hp 14 nm template has been fabricated by a self-aligned double patterning (SADP) on a template. Using this template, we have fabricated hp 14 nm dense Si lines with a depth of 50 nm on a 300 mm wafer [1].

On the other hand, in order for NIL to become standard in the near future, several issues are still remained. A chemical mechanical polishing (CMP) technology is a must for adapting NIL to the actual product wafer having dust and the step-height [2]. In addition, it is important to improve the productivity using advanced NIL processes like spin-coating NIL and multi-area imprint in order to increase the user base. New NIL-specific application, such as 3D patterning is also desired.

In this presentation, we report on the latest lithography performance of NIL and discuss the future of NIL.

[1] T. Nakasugi, et al., “Half pitch 14 nm direct pattering with Nanoimprint lithography”, 2018 IEEE International Electron Devices Meeting (IEDM), IEDM Technical Digest 2018, pp. IEDM18-265-268.

[2] M. Sakashita, et al., “IMPACT OF HIGH PERFORMANCE CHEMICAL MECHANICAL POLISHING FOR NANOIMPRINT LITHOGRAPHY”, International Conference on Planarization/CMP Technology 2019, Sep. 15-18, 2019, Taiwan.

Advanced modeling techniques for mask process development and verification

Michael Green[1], Romain Lallement[2], Mohamed Ramadan[1], Derren Dunn[2], Henry Kamberian[1], Stuart Seig[2], Young Ham[1]
[1]Photronics Inc., 10136 S. Federal Way, Boise, ID, USA
[2]IBM Research Division, 257 Fuller Rd, Albany, New York, USA

Mask technology is key to enabling the progression of advanced IC technology nodes into the realm of 5nm logic. In particular, extreme ultraviolet lithography (EUVL) relies heavily on the mask in order to achieve adequate process window (PW) and final yields. In the EUVL environment, mask process development and verification becomes increasingly more difficult and costly. The mask manufacture costs are driven by multiple factors including significantly more expensive mask blanks and increased ebeam write times. Wafer verification of mask process improvements is very difficult with the relatively low number of early adopters of EUVL and high cost associated with processing non-product wafers with that technology. It is therefore useful for mask manufacturers and wafer lithographers to collaborate to develop low cost mask process screening techniques as a precursor to committing valuable EUV exposure time for final verification. Previously, we demonstrated that by utilizing a toolkit of mask and wafer analytical techniques known as advanced mask characterization and optimization (AMCO), we were able to predict wafer defectivity on 1D and 2D metal structures and optimize a mask process to enable 30nm pitch interconnect in a single exposure step using EUVL [1]. In this study, we use similar methodology to develop a mask process for 5nm logic contact and via layers. These structures pose a different set of challenges than the metal layer. Contact hole area loss, corner rounding (CR), and mask process-induced x-y error on asymmetric holes must be optimized to deliver the required capability. Additionally, sub-resolution assist features (SRAFs) become relevant at this node. Resolving these on the mask is critical. Here, we describe the development of a mask process to overcome these challenges. We use advanced modeling techniques including AMCO to characterize the process improvements and predict wafer performance. Mask process improvements that are characterized include both physical mask process components as well as write data optimization techniques, i.e. mask process correction (MPC).

Key Words: extreme ultraviolet lithography (EUVL), advanced mask characterization and optimization (AMCO), corner rounding (CR), mask process correction (MPC)

[1] C. Progler, M. Green, R. Bonam, H. Kamberian, M. Ramadan, D. Dunn, Y. Ham, Y. Choi, L. Meli, N. Felix, D. Corliss, B. Kasprowicz, “EUV Mask challenges and requirements for ultimate single exposure interconnects”, Proc. Of SPIE Vol. 10957, February 2019

DTCO in 2019: The Precious Metal Stack and the Route to Better Designs

Brian Cline and Divya Prasad
Arm Ltd.

Technology and design scaling at process nodes <20nm is becoming more challenging with every subsequent node. To overcome scaling roadblocks and maximize the performance benefits of scaling, circuit designers and process technologists work together through a process commonly known as Design-Technology Co-Optimization (DTCO). When DTCO first became necessary and popular, the MOSFET device dominated the cost and performance equations. However, in the era of multiple patterning and EUV lithography, the importance of the metal stack is quickly rising. This new paradigm has changed the face of DTCO and impacted the way we design integrated circuits.

This talk will discuss the evolution of DTCO from a device-centric regime to an interconnect-centric regime. It will introduce the current DTCO paradigm and its drivers, and then cover the resulting design implications in order of increasing complexity: from standard cells and bitcells to microprocessors and multi-core systems. Finally, the talk will conclude with a glimpse into the future and a prediction of where DTCO will go in years to come.

Challenges Facing Photolithography in Advanced Packages

Curtis Zwenger, VP, Adv Package & Technology Integration
Amkor Technology, Inc.

Over the past five decades, many life-changing technologies were made possible by the reliable, exponential growth in the performance of semiconductors. Personal computers, smart phones and electric vehicles are just a few examples. More recently, technology companies have had to work harder to create advanced new-use cases for electronic devices and systems. The continual cramming of more silicon transistors onto chips, known as Moore's Law, appears to be grinding to a halt. Fortunately, the timely rise in technological innovations within the semiconductor packaging sector is enabling the continued growth of the industry.

Historically, Moore's law addressed the complexity of simultaneously reducing costs and scaling. More recently, Moore's Law is more about economics than anything else. The limitations found in economically scaling silicon at the most advanced nodes have paved the way for newer packaging technologies to provide enhancements and address the need for improved power and electrical performance as well as reduced cost at the most advanced nodes. The continuous goal of improving performance per watt is now being addressed at the packaging level through Heterogeneous Integration (HI).

Heterogeneous Integration allows the co-packaging of different functionalities and technological complexities within the same system or module. To support this design approach, many new packaging technologies are evolving to address the need for extreme integration of disparate chip technologies across multiple product disciplines. One of the more advanced packaging technologies is High-Density Fan-Out (HDFO) that utilizes advanced photolithography techniques to achieve high levels of integration. HDFO packages are moving toward more complex structures with finer routing layers, all requiring more capable lithography equipment and other tools. By achieving such critical features, HDFO packages will provide better performance. However, there are several manufacturing and cost issues that continue to challenge these advanced photo-defined routing structures. This presentation will discuss the challenges facing photolithography in advanced packages, such as HDFO, and explain what the packaging industry is doing to address these challenges.

Key Words: Advanced packaging, photolithography, High-Density Fan-out (HDFO), Heterogeneous Integration (HI), Moore's Law

Session 9

Presentation Schedule for
Thursday, November 7, 2019

Session Chairs
David Fried
Kafai Lai

	Time	Presenter	Title
Session 9	8:00 – 8:50 AM	Scotten Jones	***Plenary Talk: Economics in the 3D Era***
	8:50 – 9:15 AM	Yuki Watanabe	Deep learning in lithography applications
	9:15 – 9:40 AM	Daan Slotboom	EUV-DUV matching in a world of 2nm overlay
	9:40 - 10:05 AM	Toshiyuki Hisamura	ACAP – Adaptive Compute Acceleration Platform and the Lithography Needs
	10:05 – 10:35 AM	BREAK	

Economics in the 3D Era

Scotten W. Jones, President, IC Knowledge LLC

As classic 2D scaling has slowed we are seeing the industry turn to the third dimension. NAND has already successfully transitioned from 2D to 3D with over 90 stacked memory layers in production and continued increases to hundreds of layers are projected. Logic has also transitioned from planar devices to FinFETs with Horizontal Stacked Nano-Sheets and eventually CFETs on the horizon. DRAM has moved capacitor structures into the third dimension and there continues to be a search for additional 3D DRAM scaling opportunities.

In this presentation I will present projected roadmaps for the next decade for all three product types and explore projections of the resulting costs and challenges. For example, for 3D NAND even if the technical challenges can be overcome to produce several hundred layers there appears to be an economic limit. I will also explore opportunities for partitioning functionality between separate die (chiplets) as an additional cost saving.

Deep learning in lithography applications

Yuki Watanabe, Tetsuaki Matsunawa, Kenji Konomi and Shigeki Nojima
Kioxia Corporation, Memory Div. Memory Design Dept. III, Memory Lithography Group

As semiconductor devices shrinking, accurate lithography simulation techniques are required. Recently, many machine learning based approaches have been proposed to improve accuracy and computing time of lithography simulation. Machine learning is a technique to build a function which can predict output data Y from input data X. Especially, deep learning techniques, such as convolutional neural network (CNN) and generative adversarial network (GAN), are expected to make a great achievement. The effectiveness of CNN and GAN based approaches has been studied in several lithography applications, such as hotspot detection, compact resist modeling and inverse lithography technology [1]-[4].

However, an accurate prediction cannot be achieved without an appropriate definition of relationship between X and Y [5]. In addition, prediction accuracy for unknown data becomes drastically worse when the variations of the data have not been covered sufficiently in the training phase. Therefore, it is important not to rush to machine learning blindly but to discuss whether machine learning is suitable for the application.

In this presentation, we will discuss the details of the above issues.

[1] Haoyu Yang et al., “Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning”, IEEE/ACM Design Automation Conference, 2017.

[2] Yuki Watanabe et al., “Accurate Lithography Simulation Model Based on Convolutional Neural Networks”, SPIE Advanced Lithography Conference, 2017.

[3] Yibo Lin et al., “Data efficient lithography modeling with transfer learning and active data selection”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018.

[4] Haoyu Yang et al., “GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets”, IEEE/ACM Design Automation Conference, 2018.

[5] Tetsuaki Matsunawa et al., “Lithography hotspot candidate detection using coherence map”, SPIE Advanced Lithography Conference, 2019.

EUV-DUV matching in a world of 2nm overlay

Daan Slotboom
ASML Netherlands B.V.
De Run 6501, 5504 DR Veldhoven,
The Netherlands

EUV lithography is moving into volume production for 7-nm and 5-nm logic devices and will reduce the manufacturing complexity by minimizing the amount of pattern splits for critical layers. The edge placement error (EPE) requirements scale with the technology nodes, but as we discussed in a previous paper [1], the overlay requirements scale stronger in order to allow more room for stochastics in the total EPE budget.

To obtain the best possible edge placement error both Overlay and OPC are over scaled, therefore the overlay performance requirements becomes even more strict, it needs to be met in a mix-and-match mode of EUV, dry and immersion DUV. This requires systems to be set up against a common reference and needs special attention to match some of the hardware components in these platforms. On top of this higher order field to field corrections are needed on both DUV and EUV platforms to bring the overlay fingerprints closer together.

In this paper we will explain the overlay matching characteristics of DUV and EUV scanners for 3-nm logic and beyond with sub 2-nm EUV-DUV matched requirements and describe a strategy using high order correction capabilities to minimize the overlay errors between these tool types. The increase of degrees of correction, in principle requires more metrology to characterize the high spatial variation in the fingerprint, and therefor also the metrology approach will be discussed. And ultimately how these link back to the EPE budget and its components.

References:

[1] Jan Mulkens et.al., “Holistic Approach for Overlay and Edge Placement Error to meet the 5-nm Technology Node Requirements”, Proceedings SPIE Volume 10585, (2018)

ACAP – Adaptive Compute Acceleration Platform and the Lithography Needs

Toshiyuki Hisamura
XILINX, 2100 Logic Drive, San Jose, CA 95124, USA

In the emerging era of big data and artificial intelligence requiring massive computing power, Field Programmable Gate Arrays (FPGAs) has been focused as one of hardware acceleration platform. Adaptive Compute Acceleration Platform (ACAP) that goes far beyond the capabilities of an FPGA is a highly integrated multi-core heterogeneous compute platform that can be changed at the hardware level to adapt to the needs of a wide range of applications and workloads. An ACAP's adaptability, which can be done dynamically during operation, delivers higher levels of performance and performance per-watt than conventional computing platforms.

The adaptability of ACAP is fully supported by software and the hardware evolution involving both “Moore’s Law” extension to achieve higher integration at chip level and “More Than Moore” based on advanced packaging adoption to achieve higher integration at system level.

In this talk, we will review challenges to extend higher integration at chip level by EUV Lithography adoption to future nodes and also new lithography requirements to adopt advanced packaging technologies to achieve higher integration at system level from design house point of view.

Session 10

Presentation Schedule for
Thursday, November 7, 2019

Session Chairs
Bryan Kasprowicz
Sterling Watson

	Time	Presenter	Title
Session 10	10:35 – 11:00 AM	Chris Mack	Metrology for Roughness and Stochastic Variability Measurements and Why it is Essential for Making EUV Successful
	11:00 – 11:25 AM	Doug Resnick	Matching in a world of 2nm overlay
	11:25 – 11:50 AM	Martin Burkhardt	Investigation of mask absorber induced image shift in EUV lithography
	11:50 AM – 12:15 PM	Rahul Lakwawat	Optical Inspection for EUV ADI Defectivity
	12:15 - 12:40 PM	Peng Liu	Mask Synthesis using Machine Learning Software and Hardware Platforms
	12:40 PM	End Session - Lunch provided	

Metrology for Roughness and Stochastic Variability Measurements and Why it is Essential for Making EUV Successful

Chris A. Mack
Fractilia, LLC, Austin, TX

Stochastic-induced roughness continues to be one of the major concerns for EUV lithography. Stochastic effects can reduce the yield and performance of devices in several ways:

- Within-feature roughness can affect the electrical properties of a device, such as metal line resistance and gate leakage;
- Feature-to-feature size variation caused by stochastics (also called local CD uniformity, LCDU) adds to the total budget of CD variation, sometimes becoming the dominant source;
- Feature-to-feature pattern placement variation caused by stochastics (also called local pattern placement error, LPPE or local edge placement error, LEPE) adds to the total budget of PPE and EPE, sometimes becoming the dominant source;
- Rare events in the tails of the distributions of errors are more probable if those distributions have fat tails, leading to greater than expected occurrence of catastrophic bridges or breaks (or merged or missing holes and pillars);
- Decisions based on metrology results (including process monitoring and control, as well as the calibration of OPC models) can be poor if those metrology results do not properly take into account stochastic variations.

For these reasons, proper measurement and characterization of stochastic-induced roughness and defectivity are critical. Unfortunately, current roughness measurements (such as the measurement of linewidth roughness or line-edge roughness using a critical dimension scanning electron microscope, CD-SEM) are contaminated by large amounts of measurement noise caused by the CD-SEM. This results in a biased measurement, where the true roughness adds in quadrature with the measurement noise to produce an apparent roughness that is larger than the true roughness. Further, these biases are dependent on the specific CD-SEM tool used and on its settings.

In this study, a new technique for producing unbiased estimates of roughness parameters will be used to investigate the impact of roughness in EUV lithography. It is based on the use of an analytical model for SEM scattering behavior that predicts linescans for a given feature geometry. Run in reverse, an Inverse Linescan Model can be used for edge detection in such a way that SEM noise can be adequately measured and statistically subtracted from the roughness measurement, thus providing unbiased estimates of the roughness parameters. In turn, these unbiased roughness measurements will be used to make predictions about within-feature roughness, LCDU, LPPE, LEPE, and catastrophic failures for device features at the 5-nm node and below.

Matching in a world of 2nm overlay

Douglas J. Resnick
Canon Nanotechnologies Inc., 1807 West Braker Lane, Bldg. C-300 Austin, TX 78758 USA

Overlay budgets play a large role in defining production readiness. As an example, DRAM devices require overlay on the order of 20% of the half pitch. Canon's nanoimprint systems use a through the mask (TTM) alignment system to measure a Moiré image anywhere in the field. This system can also record alignment errors of all fields and all marks. The data collected by the TTM system correlates very closely with an Archer measurement tool. In addition, a High Order Distortion Correction (HODC) system, which applies a heat input on a field by field basis with a DMD array has been combined with magnification actuators to correct high order distortion terms up to K30.

In a typical nanoimprint process, resist droplets are dispensed to fill all relief images on a mask and create a uniform residual resist film beneath below the imprinted features. In this work, we introduce a new method for addressing overlay distortion, in which a drop compensation pattern is applied to match wafer non-flatness and other distortions as a means for minimizing overlay errors. The concept is illustrated in Figure 1 and shows a drop pattern designed to deliberately to create a varying resist film thickness which bends the fused silica mask and compensates the distortion introduced from either the silicon wafer or the wafer chuck. In this way, Drop Pattern Compensation (DPC) can be used to address lithography related distortion errors arising from chuck induced errors, pattern induced distortions, grid errors from a scanner, stress induced distortion and imprint related mask bending errors

By applying, the existing magnification actuator system, the heat-based HODC system and DPC, it now becomes possible to induce nanometer scale distortion corrections and address mix and match overlay errors. In this paper, models describing the mask bending induced distortion will be discussed and DPC examples will be presented.

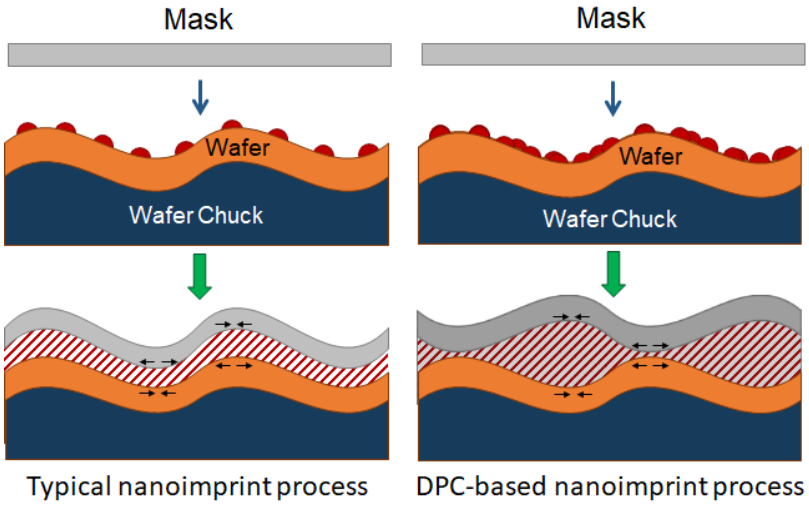


Figure 1. Left: Typical nanoimprint process. Right: DPC process, in which the residual resist film thickness is optimized to match mask and wafer bending

Investigation of mask absorber induced image shift in EUV lithography

Martin Burkhardt,[a] Anuja De Silva,[b] Jennifer Church,[b] Luciana Meli,[b] Chris Robinson,[b] Nelson Felix[b]
[a] IBM Research, Yorktown Heights, NY
[b] IBM Research, Albany, NY

With the introduction of EUV lithography into manufacturing, the lithography community still struggles with some imaging issues, like the magnitude of usable depth of focus, and reduced contrast which can impact stochastic effects such as defectivity and line edge roughness. In recent years EMF mask effects and their impact on best focus shift in EUV lithography were investigated, and alternative absorber stacks were proposed in order to improve control of focus and contrast. Recently, interest in phase shifting masks has resurfaced, and there are proposals for alternative absorber stacks that depend on feature type to be patterned.

The phenomenon that for a dipole the separate images of the two monopoles do not overlap with each other will be investigated. The contrast for the dipole is measurably lower than that of the individual monopoles. The impact of this effect on contrast and usable depth of focus will be discussed, and a method to measure this image split effect will be proposed, along with absorber materials to reduce this effect and possible techniques to counteract it on the exposure tool.

One approach to suppressing the image split has been the choice of a material that is index matched to vacuum, which therefore shows a negligible image split behavior. While this image split is indeed largely suppressed for absorbers with n close to 1, those materials have markedly low intrinsic image contrast, making them unsuitable as absorbers. Instead, we have converged on absorbers that create either a significant phase shift or feature very strong absorption, with recent proposals coming close to a π phase shift for attPSM. It is likely that the close index match to vacuum is detrimental to imaging because a larger part of the light is absorbed which would otherwise have contributed to imaging.

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Optical Inspection for EUV ADI Defectivity

Rahul Lakhawat, Annie Zhang, Kaushik Sah, Shubham Kumar, Raghav Babulnath,
Vidyasagar Anantha, Hari Pathangi & Andrew Cross

KLA Corporation

EUV Lithography since its inception has faced a lot of challenges. Starting from mask contamination to stochastics, the list of challenges is very long [1]. The current paper focuses on three key challenges: a) EUV ADI print check b) EUV ADI defectivity for CAR (Chemically Amplified Resist) & MOR (Metal Oxide Resist) and c) EUV ADI stochastics defectivity. In this paper, we demonstrate hardware, software and algorithms innovations on the KLA's 39xx Broadband Plasma platform to offer HVM friendly solutions to the above challenges.

We will discuss how innovative algorithms on 39xx can enable detection of critical reticle defects and is helping with detecting yield critical mask defects. 39xx's capability to detect sub 20 nm critical defects on both CAR and MOR resist will be demonstrated. This paper will also showcase 39xx's capability to not only detect EUV stochastic defects but also extend the stochastics studies to lower than ppb (parts per billion) defect density. Line/space and contact holes structures patterned using EUV Lithography at challenging pitches compatible with foundry N5 device node were used as a test vehicle for these studies [2].

References

[1] J Harry et al., International Conference on EUV Lithography. (2018), Vol. 1080903.
[2] R Kim et al., Proc. SPIE Vol. 10588 (2018), 105880N.

Mask Synthesis using Machine Learning Software and Hardware Platforms

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Abstract

Recent advances in machine learning (ML) algorithms have enabled many new and improved capabilities across a wide spectrum of artificial intelligence (AI) applications. The examples include image recognition, autonomous driving, cyber surveillance, virtual personal assistants, etc… These AI applications are being fueled by advanced ML software and hardware platforms that are made easy to access for all types of users. It is not surprising that lithography engineers in the semiconductor industry are also applying the ML techniques to solve challenging problems in the area of computational lithography. ML-based 3D mask modeling, resist modeling, as well as optical proximity correction (OPC) applications have been reported recently. The success and wide use of various AI applications are also promoting rapid developments in ML software and hardware platforms. For example, popular open-source ML frameworks such as TensorFlow, PyTorch and CNTK are actively developed by Google, Facebook and Microsoft respectively. In addition to CPU machines, they can also run on GPU machines for hardware-accelerated computation. New hardware dubbed as AI chips are being developed as well by both established companies and young startups to accelerate ML-based operations. In this work, we explore the possibility of taking advantage of this new ecosystem for mask synthesis applications. Specifically, we seek to run the entire mask synthesis flow in TensorFlow with GPU acceleration. We will discuss the readiness of various components including ML-based mask, optical and resist models, as well as ML-based correction engines. We will also highlight challenges that we must overcome in order to achieve the ultimate goal.

Session 11

Presentation Schedule for
Thursday, November 7, 2019

Session Chairs
Bernd Geh
Martha Sanchez

	Time	Presenter	Title
Session 11	1:40 – 2:05 PM	Clemens Utzny	Application of machine learning methods to lithographic problems
	2:05 – 2:30 PM	Joe Ervin	Assessment of Various Patterning Integration Options Using Virtual Fabrication
	2:30 – 2:55 PM	Peter Buck	Machine Learning Guided Curvilinear MPC
	2:55 - 3:20 PM	J. Alexander Liddle	Bottom-up fabrication: Promises and Pitfalls
	3:20 PM	End of session	

Application of machine learning methods to lithographic problems

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There are popular landmarks where machine learning algorithms have recently proven their prowess in mastering domains of human intelligence. The first hallmark of this type is most likely the victory of the chess computer “Deep Blue” against the then reigning world chess champion Gary Kasparov. Chess with its 8x8 fields and 32 counters is a game of simple rules with an immense complexity. This complexity results out of the vast amount of legal chess positions (around 1040) which result of the movement patterns of the counters. The game is a game of perfect information, which means that each player is informed of all the events that have previously occurred, including the "initialization event" of the game. In the case of Chess, the optimal game strategy could in principle be computed by both players at any stage of the match. However, such a computational task is beyond the abilities of humans and task is in certain situations replaced by the perception and analysis of patterns and power lines. The vast number of possible chess positions is the reason why Claude Shannon proposed in the year 1950 that in setting up a computer for Chess the simple forward computation of all possible moves should be supplemented by a selection process. In the case of “Deep Blue” the massive computational power was supplemented by a large Grandmaster game database. This combination constituted the base for selection of valid moves for “Deep Blue”.

This victory, however, was at that time only partially considered as a machine learning success, as no learning mechanism was implemented in the set up. Thus, the ancient game of Go with the substantially more legal positions of 2.08*10170 was considered as a real litmus test for machine learning. In 2015 the general believe was that it would take another 5-10 years for having a computer with enough power to win against a reigning Go champion. This estimate was based on the assumption that the software would be set up in a manner similar to “Deep Blue”. As it turned out the 9th Dan holding Go player Lee Sedol lost to the Go machine “AlphaGo” in 2016. The key points in the “AlphaGo” set up are a Monte Carlo tree search guided by a value & policy network implemented using a deep neural network technology as well as constant learning cycles of the software.

In this paper we present the architectural set up of a machine learning algorithm which successfully deals with the demands and pitfalls of mask manufacturing. A detailed motivation of this basic set up followed by an analysis of its statistical properties is given. The machine learning set up for mask manufacturing involves two learning steps: an initial step which identifies and classifies the basic global CD patterns of a process. These results form the basis for the extraction of an optimized training set via balanced sampling. A second learning step uses this training set to obtain the local as well as global CD relationships induced by the manufacturing process.

Assessment of Various Patterning Integration Options Using Virtual Fabrication

Benjamin VINCENT, Joseph ERVIN
Coventor

In this presentation, we will review the use of semiconductor Virtual Fabrication technology to support development of advanced patterning solutions at future logic nodes. We will discuss virtual methodologies to reduce the experimental burden of solving difficult lithography problems. Three different studies will be presented in the talk, each having a specific problem statement and solution.

The first study will demonstrate how Virtual Fabrication can confirm results obtained from unforeseen fab metrology data, specifically the benefit of thicker resist improving 23nm wide Via LCDU (Local Critical Dimension Uniformity) after both development and etch inspection.

The second study focuses on self-aligned-quadruple-patterning (SAQP) integration assessment for 16nm half-pitch metal line patterning. After a detailed calibration of the virtual model with Si cross section data, patterning failure rate is estimated by virtually introducing process variation in the SAQP process sequence. We will then demonstrate an Advanced Process Control solution for making SAQP more robust.

The last study demonstrates how virtual fabrication can help benchmark two different process options for block (line cut) patterning of 10nm half-pitch lines prior to wafer start. We quantify the patterning yield improvement for a self-aligned patterning approach as compared to a non-self-aligned approach using different process variation assumptions.

Machine Learning Guided Curvilinear MPC

Malavika Sharma[a], Bhardwaj Durvasula[a], Nageswara Rao[a], Ingo Bork[b], Rachit Sharma[a], Kushlendra Mishra[a], Peter Buck[c]

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ABSTRACT

At the 2018 Litho Workshop we presented a full-layout curvilinear ILT OPC flow from OPC through fracture and introduced a curvilinear MPC approach that solved the fundamental problems dealing with non-Manhattan polygons. We predicted runtime based on conventional iterative edge movement approaches and observed that while the accuracy of the solution was acceptable the runtime was too long to be practical due to the larger number of iterations required to achieve convergence. We proposed that a Machine Learning approach could be applied to reduce runtime to something reasonable.

Continuous efforts have been made by the computational lithography community to employ solutions from the ever evolving machine learning technology. Machine learning based solutions have been proposed for a variety of problems like mask making proximity effect correction, model based OPC, ILT and hot spot detection. In this work we present a neural network based solution which predicts a smart pre-bias for curvilinear features, leading to faster convergence of the MPC correction engine.

Bottom-up fabrication: Promises and Pitfalls

J. Alexander Liddle,* Michael Zwolak, and Jacob Majikes
National Institute of Standards and Technology

The term "self-assembly" encompasses a wide range of materials and processes and self-assembly methods have been explored for many years, driven by the promise that they can overcome the challenges of feature size/density and stochastic variability facing conventional, top-down lithographic approaches. Techniques such as atomic layer deposition and etching (ALD/ALE) are part of mainstream manufacturing, and self-aligned sidewall-spacer methods have been standard for a long time. One reason for the success of these approaches is that they make use of small molecular units that have very high driving forces for assembly (reaction). The high number density per cubic nanometer, coupled with careful control over nucleation and growth processes, enable sub-nanometer fabrication precision and essentially eliminate the possibility of stochastic defects [1].

Larger, more complex molecular units offer the potential both for fabrication with atomic precision over extended areas and an increased level of functionality either as a result of built-in capability, or by acting as carriers of functional objects such as quantum dots, nanoparticles, and nanotubes. However, two major challenges must be overcome to realize this potential. The first is the production of a defect-free population of molecular assemblages, and the second is to devise methods that enable them to be integrated into functional systems with minimal defectivity.

Unlike the formation of Al_2O_3 in ALD, the yield of correctly-formed supra-molecular structures, such as DNA origami, is determined by a sequence of concatenated cooperative chemical equilibria that each have finite equilibrium constants. The consequence of this is that a large fraction of the assemblies is defective. Biological systems employ an extensive and sophisticated quality control system to identify and rework or destroy defective structures [2]. While no such system currently exists for DNA-based constructs, I will describe potential approaches that may enable removal of incorrectly-assembled constructs as a first step in developing a new nanofabrication paradigm.

The incorporation of Al and O into an ALD film is highly constrained by the nature of the respective chemical bonds. Larger structures like DNA origami have many more degrees of freedom, and their accurate and precise placement necessitates careful control over the forces guiding them to avoid kinetic traps. Even though significant progress has been made in addressing this problem [3], much remains to be done. Taken together, the limitations in yield and placement/orientation accuracy and precision constrain the application space for these emerging approaches. I will comment on the need to choose the right application space for the initial introduction of the next generation of self-assembly fabrication methods.

[1] *Atomic Layer Deposition: An Overview*, S. M. George, *Chem. Rev*., **110**, 111–131 (2010)
[2] *Protein folding and misfolding*, C. M. Dobson, *Nature*, **426** 884 (2003)
[3] *Absolute and arbitrary orientation of single molecule shape*s, A. Gopinath *et al., arXiv:1808.04544*

*liddle@nist.gov

Session 12

Presentation Schedule for
Thursday, November 7, 2019

Session Chairs
Lars Liebmann
Kamal Yadav

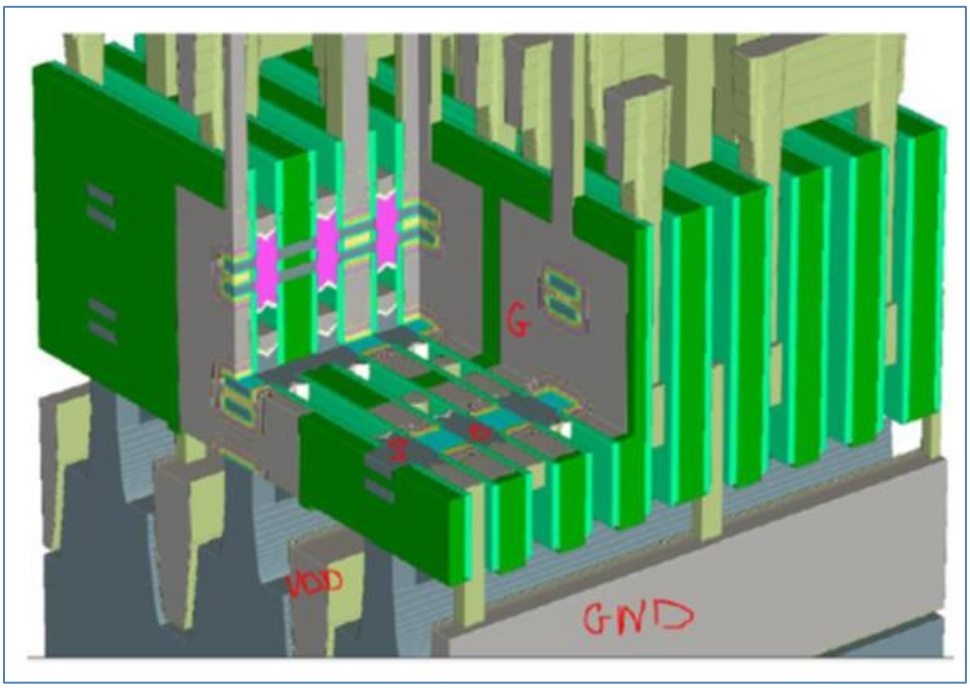
	Time	Presenter	Title
Session 12	3:30 – 3:55 PM	Jeffrey Smith	Here there be dragons – what lies at the end of the area scaling roadmap
	3:55 – 4:20 PM	Pieter Weckx	Scaling solutions in the 3rd dimension
	4:20 – 4:45 PM	Henry Kamberian	EUV Mask Technology: Challenges and Opportunities on Path to N3 Requirements
	4:45 - 5:10 PM	John Randall	The Next Generation of Ultra-High Resolution E-Beam Lithography
	5:10 – 5:25 PM	Closing Remarks	
	5:25 PM	End Session and Conference	

Here there be dragons – what lies at the end of the area scaling roadmap

Jeffrey Smith, Lars Liebmann, Daniel Chanemougame, Kanda Tapily, Subhadeep Kal, Anton deVilliers
Tokyo Electron

Logic scaling is about to get very interesting! After 30 years of scaling through lithography-driven pitch reduction and the recent incorporation of DTCO, leading-edge technology has finally reached the point at which single FIN devices with the absolute minimum number routing tracks are the current state-of-the-art. Further area scaling now needs to extend into the third dimension where truly innovative device, process, and materials innovations are being called upon to maintain the relentless pace of functional integration that has become the lifeblood of civilized existence.

The push for three dimensional devices literally opens up a whole new world of options for continued device scaling; all of which pose significant opportunities and challenges from design and module integration perspectives. In this talk we will look in depth at the integration challenges facing this push towards 3D logic devices, and how agile PPAC modelling can be incorporated to quickly explore the viable paths for module and hardware development. We will also discuss how many of these solutions which enable 3D logic devices can also be used as performance and power scaling boosters to existing 2D devices.



Scaling solutions in the 3rd dimension

Julien Ryckaert and Pieter Weckx
Imec Belgium

As logic scaling is losing steam due to limitations in patterning and device performance, 3D logic is seen as an avenue to further extend density scaling. In this talk we will evaluate the potential of exploiting the 3rd dimension to enable continuous Moore's Law scaling. Moreover, moving to a 3D architecture, a paradigm change is needed where system-technology co-optimization will be required. Technology hybridization will become the key element to partition the system. We will go through various examples of technology solutions that provide 3D scaling for Logic systems. At device level, we will review how finFET and GAA have appeared as first attempts of 3D optimization of devices. Then we will explore how CFET and VFET can potentially further scale CMOS devices structurally. We will then look at block level scaling with Sequential 3D processing and functional backside wafer process.

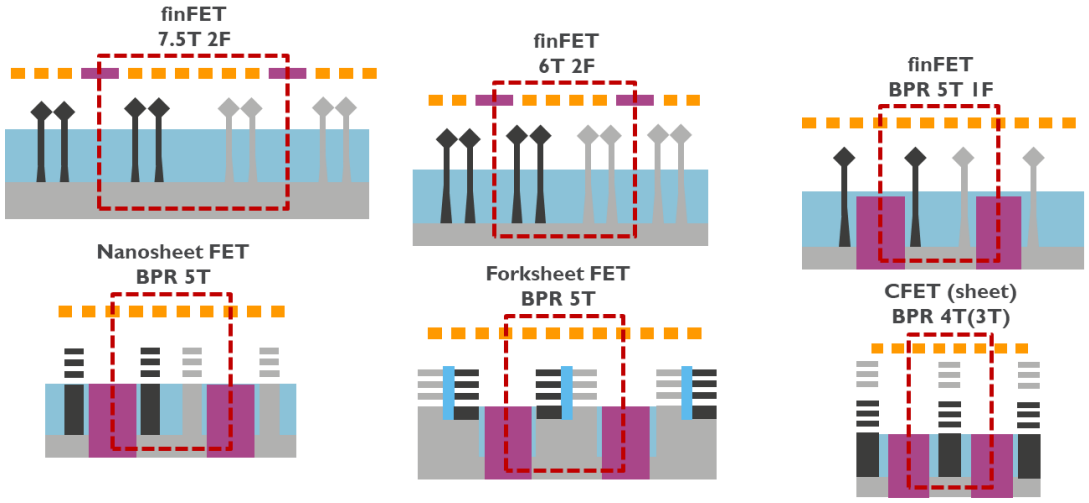


Figure 1. Device architecture migrating towards efficient use of the 3rd dimension

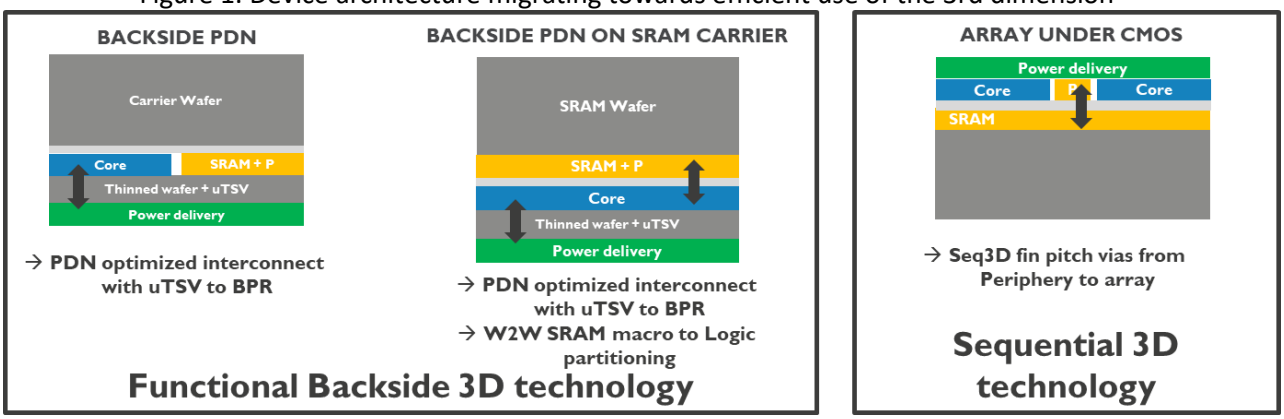


Figure 2. System-technology co-optimization to support CMOS scaling

EUV Mask Technology: Challenges and Opportunities on Path to N3 Requirements

Henry Kamberian, Daniel Lawrence, Chris Kossow, Michael Green
Photronics Inc.

Industry has made significant progress advancing EUVL technology the past several years leading to its full adoption for N7 node production. Meanwhile, challenges do remain in the EUV mask manufacturing flow from mask blank, patterning, inspection, defect repair, and defect printability. To extend EUVL technology well into 3nm node and beyond, new high-NA EUV platforms are needed. These new EUVL scanner platforms plan to use anamorphic optics with 0.55NA, which introduces several additional mask related imaging complications along with added mask manufacturing challenges. Furthermore, with these new 0.55NA systems using < 6° incidence light, absorber thickness, and non-uniform mirror reflectance through incidence angle, creates mask-induced imaging aberrations, known as Mask 3D effects (M3D). Additionally, these high NA systems will have non-telecentricity, which has shown to cause H-V bias due to shadowing, pattern shift through focus and image contrast loss due to apodization by the reflective mask coatings. All these factors point to the need of new alternate thinner absorber materials, which will dramatically reduce these effects. These new absorber materials must not only meet the improved imaging criteria, but must also meet required material properties, which makes its compatibility with different aspects of mask blank and mask manufacturing processes very critical.

In this talk, we review our advanced look into the N3 mask technology requirements from mask patterning perspective with primary focus on alternate thin absorber material. We began material evaluation and characterization studies looking into finding viable alternative thin absorbers materials, which can meet imaging requirements for these high NA platforms. While we considered and evaluated number of materials, we narrowed our focus to one unique high-k composite material, which could simultaneously meet critical requirements of low EUV reflectivity, fast etching rate and high cleaning durability. We will show preliminary results from various mask process modules testing of this new alternate thin absorber material studying modules from absorber etch, e-beam patterning, post-exposure processing and cleaning, and finally defect inspection.

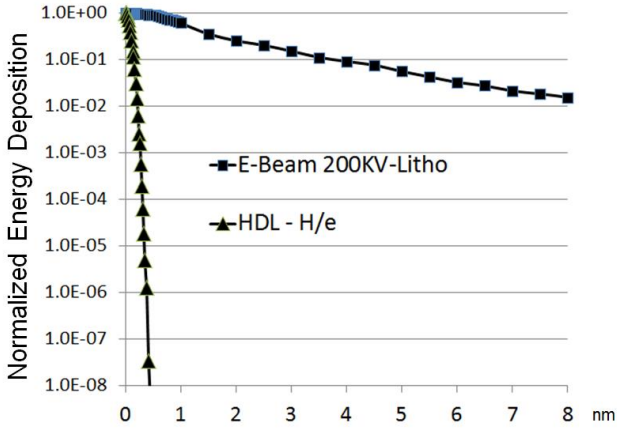
The Next Generation of Ultra-High Resolution E-Beam Lithography

John N. Randall, James H.G. Owen, and Ehud Fuchs
Zyvex Labs, Richardson Texas 75081

Conventional Electron Beam Lithography (CEBL) using scanned, focused, high-energy electron beams exposing a thin layer of polymeric resist are near their fundamental limits in resolution, precision, and throughput. The point spread function and proximity effects permit single digit nm resolution but poor relative precision. Throughput is limited primarily by space charge effects which are difficult/impossible to correct due to stochastic processes.

However there is a very different form of electron beam lithography (e-beam litho) invented in the 1990s by Lyding and Avouris which is now called Hydrogen Depassivation Lithography (HDL). It is e-beam litho because it scans a small spot of electrons across a substrate and exposes a resist. However the beam's energy, current, optics, scanning method, and resist are all significantly different. HDL is performed in Ultra High Vacuum (UHV) at room temperature with Scanning Tunneling Microscope (STM) instrumentation using a cold field emitter (the STM tip) as an electron source. The resist is a monolayer of H atoms absorbed on a single crystal surface (Si (100) 2x1) which is self-developed by the electron beam emanating from the tip. The energy difference between the lithography and imaging modes permits inspection of the Si surface before and after lithography without disturbing the resist. This fact also permits a major advantage of HDL to be developed as a digital lithography with an address grid (the Si surface lattice) and the choice of a 0.768nm square pixel being four surface Si atoms.

The resist exposure physics, a (multi-) electron stimulated desorption of the H atoms from the crystalline surface, along with the spot formation due to the tunneling process from the tip to the substrate, allows atomic resolution patterning and potentially absolute pattern fidelity. While the throughput is extremely low (Tennant's Law is upheld), there is no limiting space charge effect and the process is scalable through massive parallelization via arrays of MEMS scanners. While the throughput will not be useful for consumer electronics, HDL, with appropriate development, will be valuable for solid-state quantum computing devices and as a template writer for nanoimprint lithography.



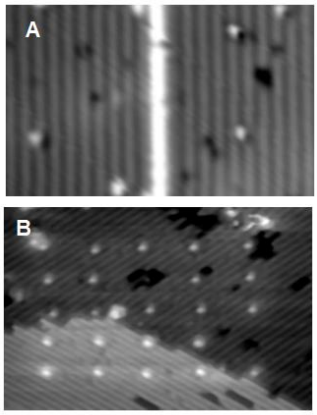


Figure 1 Normalized energy deposition of CEBL and HDL. The CEBL data was taken from Manfrinato, (2014). *Nano Letters*, *14*(8), 4406–4412.

Figure 2: HDL exposures:
A- single pixel - 0.768nm line
B- Array of individual H atoms removed.

Poster Papers

Monday, November 4, 5:00 – 7:00 PM
Tuesday, November 5, 5:00 – 7:00 PM

Presenter	Title
Alex Tritchkov	Use of Native Objective Functions in Pixel-based Mask Optimization
Derren Dunn	Title to be announced
Farhang Yazdani	Wafer/Panel level Fan-out Enabling Heterogeneous Chiplet Integration
John Peterson	Update of EUV Resist Evaluations at imec
Juhao Wu	Enhancement Cavity and Coating for Accelerator-Based EUV Sources for Lithography
Luigi Capodieci	Search and ML Applications of Pattern Matching in Lithography and DFM
Neils Wijnaendts van Resandt	Technology challenges in industrial high-speed direct write lithography
Ofir Sharoni	Excursion Prevention Strategy to increase Chip Performance by Photomask Tuning
Regina Freed	Materials Engineering Solutions to Extend DRAM Scaling
Ric Borges	Title to be announced
Shimon Levi	Title to be announced
Takahiro Mori	aquaSAVE™: Antistatic Agent for Electron Beam Lithography
Vikram Tolani	Computational Techniques Enabling EUV Mask Defect Disposition
Yuhang Zhao	AI Computational Lithography

Use of Native Objective Functions in Pixel-based Mask Optimization

Alexander Tritchkov*, Sergei Rodin, Sergey Kobelkov, Victoria Roizen, Anna Mastikhina, Yuri Granik
*Mentor - A Siemens Business, 8005 SW Boeckman Road, Wilsonville, OR 97070

Inverse Lithography Technology (ILT) has become viable RET candidate as it can produce mask output (Main Feature + SRAF) that result in process latitude and CD control in the fab, that are hard to match with conventional OPC/SRAF insertion approaches. As IC manufacturing critical dimensions become smaller, the benefit from Sub-Resolution Assist Features (SRAF) has become a must-have in DUV lithography and significant in EUV lithography. In consideration of the lithography specific effects and the critical factors and metrics to be accounted for, i.e. Edge Placement Error (EPE), Process Variability (PV Band), common Depth of Focus (cDOF), and Image Log-Slope (ILS), the DUV and EUV mask generation and optimization has become much more challenging.

An approach of solving the inverse lithography problem as a nonlinear, constrained minimization problem over a domain of mask pixels was suggested in the paper by Y. Granik ``Fast pixel-based mask optimization for inverse lithography'' in 2006. Current study extends this approach further for solving the specific print image constraints, getting maximum cDOF, minimum EPE, and keeping ILS within user specified values.

Namely, we suggest several objective functions that express penalty for constraint violations. Their minimization with gradient descent methods is considered. A number of applications have been tested with ILT-based pxOPC tool for DUV and EUV metal and contacts layouts. Results are discussed showing benefits of each approach.

Wafer/Panel level Fan-out Enabling Heterogeneous Chiplet Integration

Farhang Yazdani
BroadPak Corporation, San Jose, CA

Number of initiatives and commercial products has demonstrated that a lower cost and lower power semiconductor chip maybe realized using process agnostic chiplet approach. The low power I/O interface used to enable communication among the chiplets often results in high numbers of fine pitch bumps where a suitable substrate is necessary to make the integration possible. Cost of the substrate may prevent or delay perforation of chiplet approach and the benefits it has to offer in wide range of markets and applications. Wafer/Panel level fan-out is a promising packaging technology to minimize the costs of chiplet packaging and is considered an enabling technology for heterogeneous chiplet integration. We will present opportunities and challenges to overcome to enable wide acceptance of fan-out for low cost chiplet integration including emerging substrate technologies for fine pitch integration.

Update of EUV Resist Evaluations at imec

Authors: Danilo De Simone, Geert Vandenberghe, presented by John Petersen (imec)

In the last year, the continuous efforts on the development of extreme ultraviolet lithography (EUVL) has allowed to push the lithographic performance of the EUV photoresists on the ASML NXE:3300 full field exposure tool. However, EUVL materials are deemed as critical to enable and extend the EUV lithography technology in a cost-effective manner.

In this work, we present the imec activity on EUV materials. We show the results of the best performing EUV photoresists for dense line-space pattern at 32nm pitch, dense contact holes at 36nm pitch and dense staggered pillars at Px70nm-Py40nm pitch, reporting the most critical patterning challenges for the investigated structures. We discuss manufacturing challenges as nano-failures, line-width roughness, local critical dimension (CD) uniformity, process window limitations.

Enhancement Cavity and Coating for Accelerator-Based EUV Sources for Lithography

Juhao Wu[1], Alexander W. Chao[1], Qinghong Zhou[2], Make Ying[3], Shiuh Chao[3], Hao-Wen Luo[4]
[1]SLAC National Accelerator Laboratory, Stanford University, Stanford, CA 94309, USA
[2]School of Science, Southwest University of Science and Technology, Mianyang, Sichuan 621010, China
[3]Institute of Photonics Technologies and Department of Electrical Engineering, National Tsing Hua University, Hsinchu, 30013, Taiwan
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Taking full advantages of the advanced technologies from high-average power laser and high-energy accelerator communities, accelerator-based coherent emission (ABCE) Extreme Ultraviolet (EUV) sources can reach kilowatts average power for high volume manufacturing (HVM) lithography. In such ABCE schemes, a high-energy high-quality electron bunch interacts with a high-average power tightly focused laser pulse to produce energy modulation along the electron bunch. The energy modulation is then converted into density modulation, which leads to microbunching in the electron bunch and therefore realizes coherent emission to reach very high-average power EUV source at kilowatts level. An Enhancement cavity to build up the high-average power intra-cavity field is a critical component in such ABCE schemes. Furthermore, in some ABCE schemes, such a megawatt average power laser pulse has to be very long approaching 100 nanoseconds. A theoretic model is proposed to describe the enhancement process of such pulses in a narrow linewidth (e.g. kHz level) cavity for this demand. It is shown that a comb structure in frequency domain should be considered. Numerical simulations indicate that such pulses can be enhanced sufficiently under this condition. Some experimental schematics are elaborated for realizing such a scheme with comb structure in frequency domain. This enhancement cavity can be a standard bowtie ring cavity composed of 4-pieces high-reflective mirrors whose reflection value should achieve 99.9999% each one. While the input coating mirror should have higher transmission value than the other mirrors, purposely to introduce the seed laser input into the enhancement cavity. Due to its very high intra-cavity average power, mirror's optical absorption has to be minimized to make power enhancement operation to be ever possible. For this, coating layer on the mirrors has to be carefully designed and measured. Different coating layer deposit instruments and coating absorption detectors are contrasted to final select appropriate ones to meet these specifications for the ABCE schemes. Thermal loading effects due to this high-average power could cause significant quality degradation of the intra-cavity field. Furthermore, the pointing issue for the reflective optical beam could be very severe in achieving good three-dimensional overlap between the laser field and the electron bunch, as the reflection is very sensitive to the surface deformation. Restricted by the requirements in these ABCE schemes, the system can be very sensitive to noise disturbance. Focus is on discriminating Brownian thermal noise effect in such enhancement cavity design. Fluctuations are introduced on the laser field interacting with the electron bunch to explore the range of tolerance on the Brownian thermal noise influence in the enhancement cavity. The surface Brownian thermal noise can cause tiny deformation on the coating mirror, thus impacts the phase and amplitude of the reflection optical field overlapping with the electron bunch at each turn. This effect accumulates and affects the superposition of optical field interacting with the electron bunch for modulation. Limits on these noises are setup for the successful operation of such ABCE EUV sources for HVM lithography.

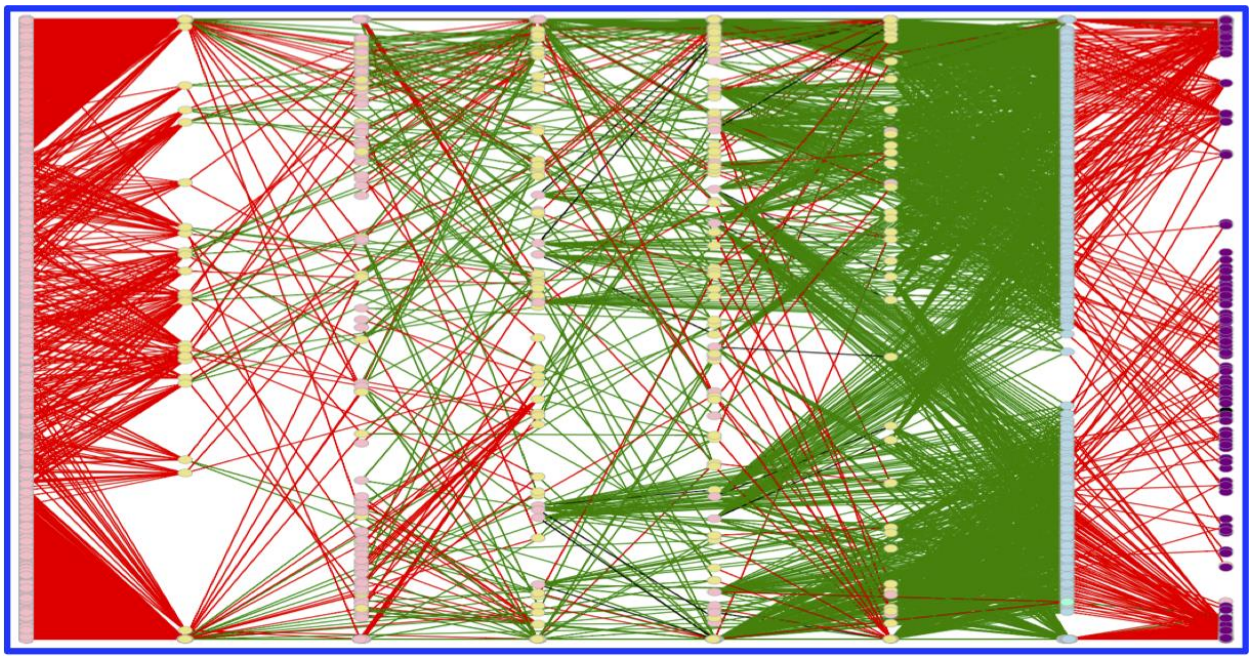
Search and ML Applications of Pattern Matching in Lithography and DFM

Luigi Capodieci[1], Vito Dai[1], Thomas V. Pistor[2], Rok Yu[2],
[1] Motivo Inc., [2] Panoramic Technology

Availability of an advanced Pattern Search Engine and a generalized formal syntax for describing, succinctly and unambiguously, all types of (multi-layer) layout patterns enables a new family of applications for VLSI layout analytics and machine learning (ML) assisted yield enhancement.

As the creation of a suitable *vector space embedding* is the first (and critical) task of virtually any ML computational flow, a library of pattern search queries generates the initial high-dimensional *point cloud data* (where each point in n-dimension represents a pattern instance). Given the extremely large cardinality of the point cloud data set, Panoramic Pattern Search introduces the flexibility of dynamic sampling the point cloud, extracting elements (i.e. generating new pattern queries) *on-the-fly*, based on the results of the previous searches. A *dynamic* point cloud, in turn, enables the use of sophisticated embedding algorithms, such as persistent homology clustering and network-graph embedding (node2vec) to extract the relevant *data features* of the original layout.

Two full-chip applications are described in this work, to exemplify both (a) the general computational framework from layout patterns, to point cloud, to vector space, to features and finally to machine learning model, and (b) how such new ML models can be used in R&D and production for DFM and Lithography. One application extracts a complete and rigorous measure (*coverage*) of layout variations, while the other application estimates *pattern similarity* and can be used to predict what type of manufacturing risk (and associated DFM correction) can be recommended for a given layout pattern (strongly analogous to Amazon™ purchase recommendations), as shown in Figure A.



[Figure A] - DFM recommendation network: generates estimated DFM fixes given input layout patterns

Technology challenges in industrial high-speed direct write lithography

Niels Wijnaendts van Resandt
Heidelberg Instruments

In recent years, when it comes to advancements in lithography, the main focus has usually been on high end photomasks or on lithography solutions for the latest node. However, there has been a growth in new applications in IoT, Automotive, Photonic IC (PIC), Sensors or 5G, that drive the demand for mature semiconductor masks at around ~1um feature sizes, often with different quality specifications.

On the other hand, while the high speed of imaging with photomasks will likely be around for a long time, there have been significant developments in direct write lithography that use fast optical modulators and high precision stages that can make maskless lithography a vailable option over mask- based lithography.

Maskless lithography could potentially offer many advantages such as eliminating the cost of acquiring, maintaining and archiving of photomask sets. For low volume production or R&D it can be of great benefit that maskless lithography allows for more flexibility by eliminating the lead-time that is involved in producing or acquiring photomasks. This could lead to a significantly shortened cycle time in development of new devices or products.

The MLA150 is an example of a highly successful Maskless Aligner (MLA) that has been widely adopted by multi-user facilities and research labs worldwide for R&D applications, but also for low volume production in commercial applications. With its use of the Texas Instruments' - DMD^{tm} micro-mirror device and automated alignment procedure it enables a high enough throughput to be an alternative to a manual mask aligner. Our further discussion will show how we built on this technology to develop the next generation tool for industrial applications that will enable even higher throughput on larger substrates (300mm) with the addition of full automation. The high flexibility of this approach will enable the flexibility required in applications such as heterogenous integration or applications where due to IP concerns the use of external photomask providers would be undesirable.

Where the high registration accuracy and the feature sizes (~500nm) of steppers are required, I will show a different approach using Grating Light Valve (GLV) technology that delivers a tool that is a direct write version of our ULTRA Semiconductor Mask Writer.

Excursion Prevention Strategy to increase Chip Performance by Photomask Tuning

Ofir Sharoni[1], Yael Sufrin[1], Avi Cohen[1], Rolf Seltmann[2], Aravind Narayana[3], Thomas Thamm[3],
[1] Carl Zeiss SMT, Bar Lev, IL, [2] RS-Lithoconsult, [3] GLOBALFOUNDRIES;

Advanced process control in lithography and overall patterning is of tremendous importance for advanced semiconductor Fabs to ensure chip performance and yield. The final patterning result and thus yield depend on many process parameters such as lithography processes, exposure tool performance, etch process, CMP etc. To control these effects various knobs, e.g. on the scanner for both wafer inter- and intra-field process control have been introduced recently, including sophisticated in-line metrology.

In this holistic lithography concept the metrology is supported by simulation and by inline data. Additionally, offline data such as the mask CDU data can be added as mask wafer interaction is also an important contribution to wafer intra-field performance. The metrology algorithm now looks for such locations where the simulation finds the weakest process features due to strong deviations of focus, dose, stage dynamics or other input parameters.

These concepts are optimized to find the sites where the process may break. Our concept of “excursion preventions” is a complimentary approach. It concentrates pro-actively on the task to minimize the distributions of critical input parameters as much as possible, independently upon a certain pre-defined specification for that parameter is met or not. In our presentation, we will describe this concept by improving wafer intra-field CDU using CD Correction (CDC) by Mask Tuning (based on wafer Intra-Filed data). Mask Tuning by the ForTune system uses ultra-short pulse laser technology to locally change the mask transmission and hence improves CDU on wafer (CDC).

To ensure a save patterning with a large enough process window without any negative yield or reliability impact, our concept looks for the tail of the final CD distribution instead of traditional 3sigma numbers. By using a calibrated 3-D resist model, we simulate the pattering result under all permutations of input parameter distributions like dose, focus and mask CDU and imaging stochastics. As a result of the simulation, we get thousands of CD-results. The tail of that CD distribution still needs to be larger the minimum CD needed for a safe etch transfer. The simulation will be additionally supported by experimental data.

Secondly, we will show in detail how the pro-active optimization of wafer intra-field CDU by Mask Tuning using the ForTune CDC process will give us more patterning margin and process stability over any other process excursion (e.g. focus deviations). Furthermore, we will present the simulated yield improvement based on the weak points (hot spots) improvement.

Materials Engineering Solutions to Extend DRAM Scaling

Regina Freed
Applied Materials

DRAM manufacturers have been on the forefront of pitch scaling and are currently mass producing some of the smallest feature pitches in our industry. To achieve these small dimensions, several techniques are being used to shrink the feature size from the best possible litho-enabled pitch to the desired device dimensions. The techniques can be collectively referred to as multi-patterning but creating the optimum patterning technique requires a good understanding of many intricate details.

All DRAM devices use a combination of techniques to scale down their dimensions, because each layer has different layout requirements and is therefore suited to specific techniques. For example, bit line and word line patterning require a technique that creates lines and spaces. For this, self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) are good options. In contacts, capacitor patterning requires the end pattern to be a circular or oval shape, which necessitates either a multi-litho process or a crisscross SADP pattern. Alternatively, EUV patterning could potentially be used, reducing the number of lithography steps required.

Independent of the technique chosen, materials engineering is used to shape, transfer, and—often—multiply the pattern. By optimizing the materials and etch processes used, significant improvements can be made to the final device performance. In this paper we will look at using materials engineering beyond the conventional approaches. What if we used materials to enable new schemes that fundamentally improve patterning cost, cycle time, and performance? One such option is a novel approach of spacer deposition and etch that creates a spacer that can be used as a mandrel. Using this approach, 4-7 process steps can be eliminated per SADP/SAQP layer. In addition, innovative multi-color schemes can be enabled by this approach, further reducing the number of process steps.

Besides cost and cycle time, minimizing local variation is essential for producing a high-yield DRAM device. Variations like overlay and critical dimension non-uniformity will create alignment or edge placement errors. To optimize for all key parameters, we used a combination of techniques. We will show that by co-optimizing materials engineering with e-beam metrology and utilizing novel data processing techniques like machine learning, an optimum patterning technique can be created that allows further scaling of DRAM devices while minimizing the processing cost.

aquaSAVE™: Antistatic Agent for Electron Beam Lithography

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aquaSAVE™ which consists of self-doped and water soluble conductive polyaniline derivatives is water-based antistatic agent. Use of this agent enables the production of thin films with excellent antistatic performance on the insulating materials. aquaSAVE™ is completely soluble in water, and has excellent filterability.

Incidentally, E-beam lithography is widely used for semiconductor scaling. E-beam lithography enables electron irradiation to any place. However, electrons accumulate on the resist surface during drawing process, E-beam is bent due to accumulation of electrons, resulting in poor placement accuracy. In order to solve this problem, accumulation of electrons can be reduced by forming Charge Dissipation Layer (CDL). aquaSAVE™ can make uniform CDL on any resists and be removed with water or water / isopropyl alcohol.

aquaSAVE™ has been used as CDL for photomask making. aquaSAVE™ has no effect of film loss and resist sensitivity for FUJIFILM PCAR. On the other hand, we have developed novel aquaSAVE™ for FUJIFLM NCAR which has achieved semiconductor scaling. As a result, novel aquaSAVE™ which we have developed for NCAR has no effect of film loss and resist sensitivity. In addition, aquaSAVE™ can reduce the electron accumulation, and then the placement accuracy is improved.

Computational Techniques Enabling EUV Mask Defect Disposition

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Even as logic chip manufacturers have committed EUV into production starting with the 7nm technology node, EUV mask inspection and subsequent defect disposition continues to be challenging, especially in the absence of any EUV actinic or high-throughput e-beam inspection platform. The 193nm optical inspectors, with substantial improvements in optical imaging, signal-to-noise and database algorithms, continue to be the workhorse for initial EUV production. To meet defect sensitivity requirements in the dense EUV mask geometries, the optical inspectors are operated rather "hot" resulting in total defect count in the thousands. Each defect in turn needs to be reviewed and dispositioned as real, nuisance or false.

Since the resolution of EUV mask patterns and defects at 193nm wavelength are generally low, it is very challenging to review defects visually without inadvertently misclassifying some real defects as nuisance. Furthermore, classified real defects are then reviewed on mask CD-SEM tools which, although slow, provide the resolution needed to better classify and characterize defect types. Subsequently, some defects, especially those that are suspected to be originating natively from the EUV blank substrate or multilayer, may also receive a high-resolution AFM scan, giving an XYZ 3D map of the defective area on the absorber. Raw data coming from the CD-SEM and AFM tools, even though high resolution, are just as challenging for operators to review and make the correct judgement call.

Computational methodologies have been developed to specifically operate on these disparate data sources and have proven to significantly help filter out nuisance detections from real ones and classify defects not only in terms of their type, for example, extrusion, intrusion, contamination, etc., but also in terms of their wafer print impact. Figure 1 shows an example data flow and the relevant computational applications that have been put into production to support manufacturability of 193nm inspections and follow-on review steps. These applications include EUV ADC (Automated Defect Classification of KLA's Teron™ 647e inspection images), S2A/S2A+ (SEM-to-Aerial for pre/post-repair characterization), and A2A (AFM-to-Aerial for native blank defect characterization).

These computational methodologies use highly advanced image, contour, and design polygon processing algorithms, die-to-database rendering of SEM and AFM reference images, EUV mask, scanner and resist modeling using PROLITH™ as-needed. Also included are user interfaces integrated with the Teron inspection tools.

Additionally, to manage all the EUV raw data collected in the mask-shop defect ecosystem, and some processed through computational applications, a next-generation high-performance and intuitive data management and analysis system is now available. This next-generation data management system links all mask, reticle and even wafer print-check defect data sources together and has intuitive reviewing, querying and defect source analysis functionalities.

The application of computational methods and effective data management for EUV defect disposition has substantially reduced loading on the follow-on repair, actinic review and/or print check down to a much

smaller subset of total defects, making the overall inspection and defect disposition flows production-worthy.

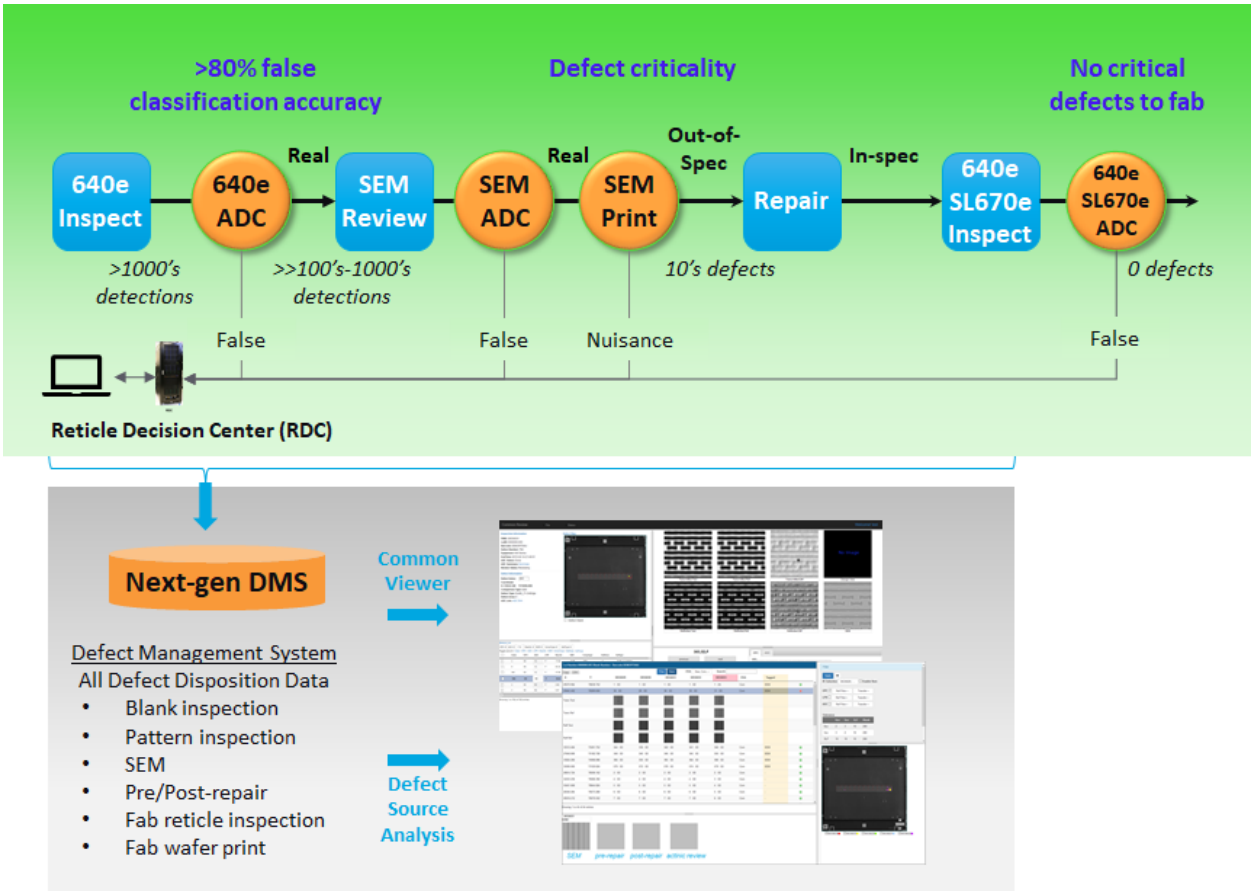

Figure 1. Comprehensive EUV mask defect disposition and data management system

AI Computational Lithography

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Abstract

With semiconductor technology progressing beyond 5nm node, there is tremendous pressure on computational lithography to achieve both accuracy and speed. One very promising technique to accomplish this mission is to take full advantage of the maturing machine learning techniques based on neural network architecture. In all machine learning based computational lithography problems, there are two aspects: the feature vector design and the mapping function construction. Mapping function construction can be realized using neural network architecture, while feature vector design must achieve optimal resolution, sufficiency and efficiency simultaneously. In this paper, we made an attempt to design physics based feature vectors, and AI computational lithography results, both OPC and ILT, will be presented. For AI OPC, the maximum error of training is around +/- 3.2nm, while the maximum error of verification is around +/- 3.5nm. For AI ILT, very promising results have also been achieved using dynamic and adaptive weighting scheme in training. It should be understood that AI based computational lithography solutions do not possess the capability to replace conventional OPC or ILT completely due to its lack of required accuracy. However, it can provide an initial solution that is close enough to final OPC solution or ILT solution, therefore fast OPC and fast ILT can be realized.

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